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#### **AMANDA**

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#### D2.1 Report on AMANDA Sensors Development

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## List of definitions & abbreviations

Definition	
Analog-to-Digital Converter	
Analog Front End	
Analog Mixed Signal	
Application Specific Integrated Circuit	
Autonomous Smart Sensing Card	
Automatic Test Pattern Generation	
Bill Of Material	
CMOS Image Sensor	
Complementary Metal-Oxide-Semiconductor	
Chip-Scale Package	
Digital to Analogue Converter	
Direct Current to Direct Current voltage converter	
Digital Camera Interface	
Discrete Fourier Transform	
Design for Test	
Dynamic Range	
Design Rule Check	
Delta Reset Sample	
Electrolyte Double Layer	
Field of View	
Frames per second	
High Dynamic Range	
Integrated Circuit	
Low Drop-out voltage Regulator	
Land grid array	
Low Power Trans Impedance Amplifier	
Layout Versus Schematics Check	
Low Voltage Threshold	
Microcontroller	
MUltipleXer	
Place & Route	
Power Amplifier	
Process Development Kit	
Power Management Integrated Circuit	
Region of Interest	
Register Transfer Level	
Schematic Driven Layout	
Signal to Noise Ratio	
Small Outline Integrated Circuit	
Serial Peripheral Interface	
Samples Per Second	
Static Timing Analysis	
Trans Impedance Amplifier	
Working Distance	
Micro Controller	

#### **Executive Summary**

The present document is a Deliverable of the AMANDA project, funded by the European Commission's Directorate-General for Research and Innovation (DG RTD), under its Horizon 2020 Research and Innovation programme (H2020).

This document reports the activities and results of **Task T2.1** – **Design and Development of AMANDA Sensors** which is part of **WP2** – **Sensor development and multi-sensorial optimisation** of the AMANDA project. Four sensors have been specifically developed in the framework of the project:

Sensor	Contributing partner
Solid-state CMOS imaging sensor	EPEAS
CO <sub>2</sub> sensor and dedicated readout system	IMEC
Capacitive touch and proximity sensor	Microdul
Solid-state temperature sensor	Microdul

Table 1 AMANDA sensors

This document describes each of the sensors in its own Section (Sections 2 to 5). The sensors' description follows a uniform structure, covering the following contents:

- Summarised in a first part are the conclusions and the derived requirements from WP1 – System Specifications, Requirements and Use Cases. These are the basis for the specifications of the four custom sensors developed within Task T2.1
- Following is a summary of the most important specifications of each of the sensors, including the main features, a block diagram, the available interfaces, configuration options & register description, an application diagram and the main electrical characteristics
- Subsequently a description of the work carried out by the contributors of the custom sensors is presented, including an overview of the obtained results
- As far as available, first evaluation results of the fabricated sensor are presented. Also, an outlook to the coming full evaluation is given
- The last part presents the physical details of the both, the sensor prototypes and the final miniaturized sensor packages. This information is required for the integration of the sensors into the initial unconstrained AMANDA hardware platform, and later into the final miniaturized ASSC

The results and status of the sensor development at the time of the completion of this report can be summarised as follows:

- 1) Image sensor. The design has been completed, and data was sent for fabrication. The factory has delayed the tape-out however by one month. Additionally, the factory accidentally destroyed some wafers and the fabrication had to be re-started. Due to these delays, the samples are expected by the end of 2020 and measurements are planned for Q1 2021. As of the 28<sup>th</sup> August, there is no confirmed date for fab-out
- 2) **CO<sub>2</sub> sensor.** Consists of the electro-chemical transducer and the electronic readout. While the mainly software-based development of the readout electronics progressed as planned, there are technical difficulties with the transducer. Different materials still need to be tested. Samples of the current sensor are available for integration into the first AMANDA prototype versions
- 3) **Capacitive sensor.** The design has been completed, the wafers have been produced and currently the prototype sample production is ongoing. First results from testing

- the samples are expected in M20, in time with the original plan, and can be provided for the integration into the AMANDA card prototype
- 4) **Temperature sensor.** The design has been completed according to schedule. The wafers are currently being fabricated. The fabrication was delayed due to a cyber-attack on the wafer fab, but the production has resumed now. First tested and calibrated samples are planned to be available on M21

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#### 1 Introduction

This document describes the development of each of the four custom developed sensors in its own Section (Sections 2 to 5). Each sensor description follows a uniform structure and covers the following topics.

#### 1.1 Objectives and requirements identified in WP1

After stating the initial objectives for the four contributed sensors for the AMANDA ASSC in the DoW, these have been taken up and refined within the frame of WP1 - System Specifications, Requirements and Use Cases. In Deliverable D1.1 - SoA and Gap analysis/recommendations on ESS features report, the current State-of-the-Art in the corresponding sensing fields has been analysed and some conclusions towards the requirements of the custom sensors for AMANDA have been drawn in the GAP analysis. During the elaboration of the system requirements and specifications, which are documented in Deliverables D1.2 - Initial system requirements specified, D1.3 - Voice-of-the Customer completed, D1.6 - Full system specification and BOM delivered, and D1.7 - Architecture design of the AMANDA system delivered (for both breadboard and integrated/miniaturised system), the requirements for the four custom developed sensors were refined and partially adapted to better suit the AMANDA application.

In this Section, the conclusions drawn from the WP1 activities are stated for each of the custom sensor developments.

#### 1.2 Sensor key specifications

This part of the description summarises the key specification properties of the sensors. It should give the reader an overview of the characteristics and the operation of device, and an impression how it can be used. For a full description of the respective sensor, the reader is referred to the datasheets already available (for example [1], [2]), or which will be published later by the individual companies.

Included in this specification overview are a feature list, a pin description, a block diagram showing the device architecture, a description of its interfaces towards the system controller, an overview of the configuration possibilities, eventually including a list of the configuration registers, a description of the most important device functions, in particular if they are relevant for the AMANDA application, and the main electrical properties and characteristics of the devices.

#### 1.3 First evaluation results of prototype sensors and evaluation planning

Full evaluation of the sensor prototypes is not part of Task T2.1. Therefore, the results cannot be presented in this report. Consequently, this Section concentrates on giving an outlook to the planned evaluations within the frame of other Tasks, like **T6.2 - Lab environment validation** and **T2.5 - Prototypes finalization**. Nevertheless, some first results will be included as they become available.

#### 1.4 Prototype samples and final miniaturized samples

The AMANDA platform is developed in stages. First, a size-unconstrained version of the ASSC is built, which allows having a system early on in the project to validate architectural decisions, to develop drivers and application software, to test algorithms, and to integrate the new sensors at an early prototyping state. For this unconstrained version of the platform, the new sensors should be delivered as early as available and only with the basic functionality checked. In most cases, the sensor chips are first assembled into prototype packages, which are easier

to handle in the lab environment, and which are faster and cheaper to produce for small quantities. For the unconstrained ASSC platform, it is also easier to integrate the prototype packages, than the final miniaturized packages (like CSP, for instance).

For the final miniaturized ASSC built towards the end of the project, the sensors must also be delivered in their final package form. This package will however only be required during year three of the project. So, there is enough time to evaluate the new sensor ICs before assembling them in the miniaturized package.

This Section presents the prototype packages and the final packages for each of the sensors in detail, including geometrical drawings, pin assignments and additional package and integration related information where applicable.

The  $CO_2$  sensor description deviates to some extent from this structure and content. While the other three sensors are CMOS solid state IC developments and can be described in a similar manner, the  $CO_2$  sensor consists of an electro-chemical sensing device and an (off-the-shelf) microcontroller, for which a signal processing algorithm is developed to extract the  $CO_2$  measurement value.

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#### 2 Imaging sensor

#### 2.1 Objectives and requirements identified in WP1

The CMOS image sensor (CIS) developed within the AMANDA project is specified following the SoA conclusions. During the last decade, huge advances have been brought to high resolution image sensors integrated into smartphones and other devices. These sensors have a very large number of pixels and technics have been developed to reach a drastic noise reduction. On the other hand, they consume large amounts of energy.

For IoT and embedded systems, the opposite trend is required: the reduction as much as possible of the power consumption by lowering the resolution and tolerating additional levels of noise.

Research exists on image sensors that work with a very low-power consumption [3] [4] [5] [6]. These CIS feature a very low energy consumption, with under 50pJ/frame/pixel and rely on the reduction of the supply voltage to lower dynamic losses. But the achievable resolution is very low and does not comply with industry standards such as VGA resolution.

To reduce power consumption, high precision ADCs cannot be used anymore to convert the light information into a digital value as they consume a lot of energy. One of the main challenges lies thus in the design of new paradigms of sensors architecture.

Based on previous work from the Université Catholique de Louvain (UCLouvain) [6] [7], EPEAS will develop a new generation, ultra-low power, time-based image sensor for the AMANDA project. These image sensors convert the light information into a pulse whose length depends on the intensity. The pulses are subsequently converted to a digital value via counters.

Compared to previous version and in accordance with recommendations done in Deliverable D1.1, this new version has several improvements (see Section 2.2.1 for more details): high dynamic range, auto exposure, edge map, region of interest, higher maximum frame rate, dead pixel correction and aggregation/decimation of pixels.

#### 2.2 Sensor key specifications

#### 2.2.1 Main features

The image sensor developed within the AMANDA project includes the following features:

- High dynamic range. A new mode has been added to extend the dynamic range: the
  high dynamic range. Rather than having a linear response to light, this mode uses multiple lines to approximate a logarithmic response (piecewise linear approximation)
- Auto exposure. When this setting is activated, the CIS will automatically update the EXPOSURE register at the end of the capture. The new exposure is calculated so that the mean luminance of the picture converges towards the mean luminance configured in the AUTOEXPTRGT registers. It should be noted that the mean luminance is only calculated on a subset of pixels in the picture. Moreover, the user can fix a minimum and a maximum value for the newly calculated exposure through the AUTOEXPMIN and AUTOEXPMAX registers. An interruption can be generated when the new exposure is clipped to one of these values
- Edge map. In this mode, the CIS will output a black and white image where the edges have been detected using the Sobel algorithm. The threshold of the algorithm is set through the EDGEMAP\_THR registers. This mode only works when the resolution is configured in QVGA or QQVGA
- Region of interest. It is possible to only capture a part of the full array. This array is divided in blocks of 32 pixels horizontally (X-axis) and 32 pixels vertically (Y-axis). When enabling ROI, the CIS will only capture the blocks comprised between the boundaries defined in the ROI start and end registers in the X and Y direction. (0,0) is the bottom left of the picture

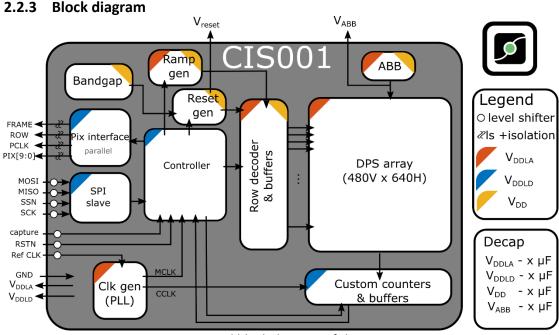
- **Higher maximum frame rate.** Compared to the baseline version, the maximum frame rate was doubled to a maximum of 16fps in delta-reset sample (DRS) mode
- **Flip.** The registers of the imager can be configured to output a flipped frame. The flip can either be in the X direction or in the Y direction
- **Dead pixel correction.** This feature allows correction of two dead pixels by replacing their values with the mean value of the neighbouring pixels in the same row (or the value of the neighbouring pixel if the dead pixel is on an end of row). The coordinates of the dead pixels are programmed through the DPO and DP1 registers
- Aggregation and decimation of pixels. In this mode, a configured number of pixels in the same line are aggregated together and only their mean value is outputted on the DCMI bus, reducing its frequency by the aggregation factor. This not is not available when the edge map is activated
- **Interruptions.** The CIS can generate interruptions based on different events. The events are:
  - o Capture done: Generate an interruption at the end of a capture
  - Exposure almost done: Generate an interruption a configured time before the end of the exposition phase (i.e. a configured time before the DCMI starts sending the data)
  - Auto exposure max: Generate an interruption when the new calculated exposure in autoexposure mode is above the configured max value for the exposure
  - Auto exposure min: Generate an interruption when the new calculated exposure in autoexposure mode is under the configured min value for the exposure
  - Auto exposure overflow: Generate an interruption when the new calculated exposure in autoexposure mode exceeds the 16-bit range of the exposure register

#### 2.2.2 Pin description

Pin	Symbol	Туре	Description
1	VDDH	Supply	IO supply + core supply
2	MISO	Output	SPI interface
3	MOSI	Input	SPI interface
4	SCK	Input	SPI interface
5	SSN	Input	SPI interface
6	VDDH	Supply	IO supply + core supply
7	GND	Supply	Ground
8	VDDLD	Supply	Supply of the digital
9	VSYNC	Output	DCMI interface - Vertical sync
10	HSYNC	Output	DCMI interface - Horizontal sync
11	PCLK	Output	DCMI interface – clock
12	CONFIG2	Input	Config bit 2
13	VDDH	Supply	IO supply + core supply
14	VDDH	Supply	IO supply + core supply

15	PIX9	Output	DCMI Interface – pixel value
16	PIX8	Output	DCMI Interface – pixel value
17	PIX7	Output	DCMI Interface – pixel value
18	VDDLD	Supply	Supply of the digital
19	VDDH	Supply	IO supply + core supply
20	GND	Supply	Ground
21	MCLK	Input	Master clock
22	PIX6	Output	DCMI Interface – pixel value
23	PIX5	Output	DCMI Interface – pixel value
24	PIX4	Output	DCMI Interface – pixel value
25	GND	Supply	Ground
26	VDDH	Supply	IO supply + core supply
27	VDDH	Supply	IO supply + core supply
28	VDDLD	Supply	Supply of the digital
29	PIX3	Output	DCMI Interface – pixel value
30	PIX2	Output	DCMI Interface – pixel value
31	PIX1	Output	DCMI Interface – pixel value
32	VDDH	Supply	IO supply + core supply
33	GND	Supply	Ground
34	PIX0	Output	DCMI Interface – pixel value
35	IRQ	Output	Interrupt
36	CAPTURE	Input	Start capture
37	RSTB	Input	Reset the chip
38	CONFIG1	Input	Config bit 1
39	VDDH	Supply	IO supply + core supply
40	VDDH	Supply	IO supply + core supply
41	RST_HIGH	Analog	Debug
42	RST_MID	Analog	Debug
43	RST_LOW	Analog	Debug
44	VABB	Analog	Debug
45	VDDH	Supply	IO supply + core supply
46	GND	Supply	Ground
47	GNDA	Supply	Clean ground of the analog part
48	GNDA	Supply	Clean ground of the analog part
49	VDDLA	Supply	Supply of the analog part
50	VDDLA	Supply	Supply of the analog part
51	GND	Supply	Ground
52	VDDH	Supply	IO supply + core supply

Table 2 Pin description table of the image sensor



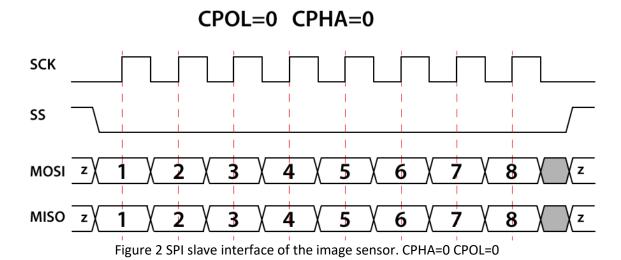
#### Figure 1 Functional block diagram of the image sensor

#### 2.2.4 Interfaces

#### 2.2.4.1 SPI slave interface

The SPI interface is used to configure the registers in the CIS. The SPI slave interface is configured to work with CPOL = 0 and CPHA = 0 configuration. It is not possible to write to registers when the CIS is taking a picture. Attempts to write a register during capture will be ignored and the MISO will return a 1 during the data phase of the SPI transfer.

Note that the value of the EXPOSURE registers can be modified by the CIS in auto-exposure mode. These registers are not synchronized when they are being read by the SPI. This means that, if the MCU tries to read them while the update is taking place, wrong values might be returned. To make sure the values are correct, either reading must be done between captures or, if reading during capture is required, reading must be done twice and it must be checked that the two values are the same.



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#### 2.2.4.2 DCMI interface

The DCMI output interface is composed of 3 control signals, and a 10-bit parallel bus. The 3 control signals are:

- PCLK: pixel clock. Values of the pixels are changed on the rising edge of this clock and must be sampled on the falling edge. The PCLK can be configured to be active at different times:
  - o Always on: PCLK is always on (if the power mode is ACTIVE)
  - Capture: PCLK is active only during the capture of an image (exposure time + transmission time)
  - o Frame: PCLK is active during transmission of an image
  - o Row: PCLK is active only when rows are transmitted. It is deactivated between rows when HSYNC is LOW. This mode is only valid in DRS mode
- VSYNC: This signal goes up at the beginning of the frame, stays up during all transmission and goes down at the end of the frame
- HSYNC: This signal goes up at the beginning of a row of pixel and goes down at the end of the row

The image is composed of all pixels transmitted when HSYNC and VSYNC are both high.

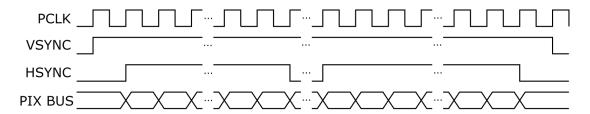


Figure 3 DCMI interface of the image sensor – always-on PLCK example

#### 2.2.5 Configuration registers

Ad- dress	Name	Bit	Field	Access	Reset	Description
0x00	CAPTURE	[0:0]	CAPTURE	W	0X0	Capture field
0x01	MODE	[3:0]	MODE	R/W	0X1	Capture mode field
0x02	PMODE	[1:0]	PMODE	R/W	0X0	Power mode field
0x03	PCLK_MODE	[1:0]	MODE	R/W	0X1	Mode field
0x04	EXPOSURE_B0	[7:0]	EXP	R/W	0XFD	Exposure field
0x05	EXPOSURE_B1	[7:0]	EXP	R/W	0X3	Exposure field
0x06	STATUS	[0:0] [1:1]	CPT SPS	R R	0X0 0X1	In capture field Switching power state field
0x07	SOFT_RST	[0:0]	RST	W	0X0	Reset field
0x0C	IRQ_EXPADCFG	[7:0]	CNT	R/W	0X0	Clock cycles left before end of exposure. The clock used is the system clock divided by 512

						(46.875 kHz for a system clock of 24MHz)
0x0D	IRQEN	[0:0] [1:1] [2:2] [3:3] [4:4]	CPTDONE EXPAD AUTOEXPMAX AUTOEXPMIN AUTOEXPOV	R/W R/W R/W R/W	0X0 0X0 0X0 0X0 0X0	Capture done field Exposure almost done field Autoexposure max field Autoexposure min field Autoexposure overflow field
0x0E	IRQFLG	[0:0] [1:1] [2:2] [3:3] [4:4]	CPTDONE EXPAD AUTOEXPMAX AUTOEXPMIN AUTOEXPOV	R R R R	0X0 0X0 0X0 0X0 0X0	Capture done field Exposure almost done field Autoexposure max field Autoexposure min field Autoexposure overflow field
0x0F	IRQCLR	[0:0] [1:1] [2:2] [3:3] [4:4]	CPTDONE EXPAD AUTOEXPMAX AUTOEXPMIN AUTOEXPOV	W W W W	0X0 0X0 0X0 0X0 0X0	Capture done field Exposure almost done field Autoexposure max field Autoexposure min field Autoexposure overflow field
0x10	ROI_EN	[0:0]	EN	R/W	0X0	Range of interest enable field
0x11	ROI_X_START	[4:0]	ROI_X_START	R/W	0X0	Range of interest X start field
0x12	ROI_X_END	[4:0]	ROI_X_END	R/W	0X13	Range of interest X end field
0x13	ROI_Y_START	[3:0]	ROI_Y_START	R/W	0X0	Range of interest Y start field
0x14	ROI_Y_END	[3:0]	ROI_Y_END	R/W	OXE	Range of interest Y end field
0x15	RESOLUTION	[1:0]	RES	R/W	0X0	Resolution selection field
0x16	LAGGREG	[2:0]	AGGREG	R/W	0X0	Aggregation field
0x17	EDGEMAP	[0:0]	ENABLE	R/W	0X0	Enable field
0x18	EDGE- MAP_THR_B0	[7:0]	THR	R/W	0X0	Threshold LSB field
0x19	EDGE- MAP_THR_B1	[0:0]	THR	R/W	0X0	Threshold MSB field
0x1A	FLIP	[0:0] [1:1]	HORIZONTAL VERTICAL	R/W R/W	0X0 0X0	Horizontal field Vertical field

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0x20	AUTO_EXPO- SURE	[0:0]	EN	R/W	0X0	Enable field
0x21	AUTOEX- PTRGT_B0	[7:0]	TRGT	R/W	0X0	Target field
0x22	AUTOEX- PTRGT_B1	[1:0]	TRGT	R/W	0X2	Target field
0x23	AUTOEXP- MAX_B0	[7:0]	MAX	R/W	OXFF	Max field
0x24	AUTOEXP- MAX_B1	[7:0]	MAX	R/W	OXFF	Max field
0x25	AUTOEX- PMIN_B0	[7:0]	MIN	R/W	0X0	Min field
0x26	AUTOEX- PMIN_B1	[7:0]	MIN	R/W	0X0	Min field
0x28	HDR_RSTHIGH_ B0	[7:0]	HDR_RSTHIGH _B0	R/W	0X7F	LSB of exposure count when to apply reset high (manual HDR)
0x29	HDR_RSTHIGH_ B1	[7:0]	HDR_RSTHIGH _B1	R/W	0X0	MSB of exposure count when to apply reset high (manual HDR)
0x2A	HDR_RST- MID_B0	[7:0]	HDR_RST- MID_B0	R/W	0X7	LSB of exposure count when to apply reset mid (manual HDR)
0x2B	HDR_RST- MID_B1	[7:0]	HDR_RST- MID_B1	R/W	0X0	MSB of exposure count when to apply reset mid (manual HDR)
0x2C	HDR_RSTLOW_ B0	[7:0]	HDR_RSTLOW _B0	R/W	0X1	LSB of exposure count when to apply reset low (manual HDR)
0x2D	HDR_RSTLOW_ B1	[7:0]	HDR_RSTLOW _B1	R/W	0X0	MSB of exposure count when to apply reset low (manual HDR)
0x30	ANALOG_GAIN	[3:0]	GAIN	R/W	0X6	Gain field
0x31	CCLK_CAL	[7:0]	CCLK_CAL	R/W	0X78	CCLK calibration field
0x32	MCLK_DIV	[2:0]	DIV	R/W	0X0	Divider field
0x33	CCLK_DIV	[2:0]	DIV	R/W	0X5	Divider field
0x34	CCLK_MUX	[0:0]	SEL	R/W	0X0	Select field
0x35	CAL_CLK_BUFF_ BO	[7:0]	CAL_CLK_BUF F_B0	R	0X0	Calibration clock buffer LSBs field
0x36	CAL_CLK_BUFF_ B1	[7:0]	CAL_CLK_BUF F_B1	R	0X0	Calibration clock buffer MSBs field

0x37	CAL_RAMP_CO UNT_B0	[7:0]	CAL_RAMP_C OUNT	R	0X0	Calibration ramp count LSB field
0x38	CAL_RAMP_CO UNT_B1	[7:0]	CAL_RAMP_C OUNT	R	0X0	Calibration ramp count middle byte field
0x39	CAL_RAMP_CO UNT_B2	[7:0]	CAL_RAMP_C OUNT	R	0X0	Calibration ramp count MSB field
0x3A	IO_DRIVE_CAL	[0:0]	CAL	R/W	0X1	Calibration field
0x3B	ABB_EN	[0:0]	EN	R/W	0X1	ABB enable field
0x40	DPCORR	[0:0]	EN	R/W	0X0	Dead pixel correction enable field
0x41	DP0_B0	[7:0]	COLLSB	R/W	OXFF	LSB column field
0x42	DP0_B1	[1:0] [7:2]	COLMSB ROWLSB	R/W R/W	0X3 0X3F	MSB column field LSB row field
0x43	DPO_B2	[2:0]	ROWMSB	R/W	0X7	MSB row field
0x44	DP1_B0	[7:0]	COLLSB	R/W	OXFF	LSB column field
0x45	DP1_B1	[1:0] [7:2]	COLMSB ROWLSB	R/W R/W	0X3 0X3F	MSB column field LSB row field
0x46	DP1_B2	[2:0]	ROWMSB	R/W	0X7	MSB row field
0x7E	TEST	[7:0]	TEST	R/W	0X0	Test field
0x7F	VERSION	[7:0]	VERSION	R	0X5	Version field

Table 3 List of configuration registers of the image sensor

## 2.2.5.1 **CAPTURE**

2.2.3.1 CALL	OIL .
CAPTURE	Capture register
Address	0x00
Reset value	0x00
Access	write-only
Fields	[0:0] – CAPTURE
	Start frame capture. During capture, it is not possible to write to the CIS
	registers
	0: NONE - W: No effect
	1: CPT - W: Start frame capture

## 2.2.5.2 MODE

MODE	Capture mode register
Address	0x01
Reset value	0x01
Access	read-write
Fields	[3:0] – MODE
	Select mode for capture
	0: SO - W: Select SO mode - R: SO mode selected

1: DRS - W: Select DRS mode - R: DRS mode selected
2: CAL_SO - W: Select SO and ramp calibration mode - R: SO and ramp
calibration mode selected
3: CAL_DRS - W: Select DRS and ramp calibration mode - R: DRS and
ramp calibration mode selected
4: TEST - W: Select test pattern mode - R: Test pattern mode selected
5: CAL_CLK - W: Select calibration cclk mode - R: Calibration cclk mode
selected
11: SO_HDR - W: Select SO HDR mode - R: SO HDR mode selected
12: DRS_HDR - W: Select DRS HDR mode - R: DRS HDR mode selected
13: SO_HDR_MAN - W: Select SO HDR mode with manual timing - R:
SO HDR mode with manual timing selected
14: DRS_HDR_MAN - W: Select DRS HDR mode with manual timing -
R: DRS HDR mode with manual timing selected

## 2.2.5.3 PMODE

PMODE	Power mode register
Address	0x02
Reset value	0x00
Access	read-write
Fields	[1:0] – PMODE
	Select power mode. Note that this field requires synchronization when
	written. Attempts to write to this register while it is still synchronizing from
	a previous access will be ignored and will return 1 on the MISO line.
	0: Active - W: Select Active mode - R: Active mode selected
	1: Standby - W: Select Standby mode - R: Standby mode selected
	2: Sleep - W: Select sleep mode - R: Sleep mode selected

#### 2.2.5.4 PCLK MODE

PCLK_MODE	Pix out clock mode register
Address	0x03
Reset value	0x01
Access	read-write
Fields	[1:0] – MODE
	Select mode for clock of the DCMI output. The 4 modes are:
	<ul> <li>Always-on: PCLK is always ON (only in active)</li> </ul>
	Capture: PCLK is only ON during capture
	Frame: PCLK is only ON during frame transmission
	Row: PCLK is only ON during row transmission
	Row mode is only valid for DRS mode. In SO, row mode behaves as frame
	mode.
	0: AO - W: Select always on mode - R: Always-on mode selected
	1: CPT - W: Select capture mode - R: Capture mode selected
	2: FR - W: Select frame mode - R: Frame mode selected
	3: ROW - W: Select row mode - R: Row mode selected

## 2.2.5.5 **EXPOSURE\_B0**

EXPOSURE_B0	Exposure LSB register
Address	0x04
Reset value	0xFD
Access	read-write
Fields	[7:0] - EXP
	LSB for exposure time selection. The exposure is expressed in clock cycles where the clock used is the system clock divided by 512 (46.875 kHz for a
	system clock of 24MHz). In SO mode the effective exposure will be
	rounded up to be equal to 3N+4 and in DRS mode to 6N+7

#### 2.2.5.6 **EXPOSURE\_B1**

EXPOSURE_B1	Exposure MSB register
Address	0x05
Reset value	0x03
Access	read-write
Fields	[7:0] - EXP  MSB for exposure time selection. The exposure is expressed in clock cycles where the clock used is the system clock divided by 512 (46.875 kHz for a system clock of 24MHz). In SO mode the effective exposure will be rounded up to be equal to 3N+4 and in DRS mode to 6N+7

#### 2.2.5.7 STATUS

STATUS	Status register
Address	0x06
Reset value	0x02
Access	read-only
Fields	[0:0] — CPT
	CIS is busy capturing an image
	[1:1] – SPS
	CIS is busy switching between power states

#### 2.2.5.8 SOFT\_RST

SOFT_RST	Soft reset register
Address	0x07
Reset value	0x00
Access	write-only
Fields	[0:0] – RST
	Soft reset of the CIS
	0: NONE - W: No effect
	1: CLR - W: Soft reset

## 2.2.5.9 IRQ\_EXPADCFG

IRQ_EXPADCFG	Exposure almost done configuration register
Address	0x0C

Reset value	0x00
Access	read-write
Fields	[7:0] - CNT
	This field indicates when the exposure almost done IRQ must be gener-
	ated (in 48kHz clock cycles before end of exposure). Acceptable values are
	bounded to min(exposure-2, 255).

## 2.2.5.10 IRQEN

IRQEN	IRQ enable register
Address	0x0D
Reset value	0x00
Access	read-write
Fields	[0:0] – CPTDONE
	Enable capture done IRQ
	0: DIS - W: Disable capture done IRQ - R: Capture done IRQ disa-
	bled
	1: EN - W: Enable capture done IRQ - R: Capture done IRQ enabled
	[1:1] — EXPAD
	Enable exposure almost done IRQ
	0: DIS - W: Disable exposure almost done IRQ - R: Exposure almost done IRQ disabled
	1: EN - W: Enable exposure almost done IRQ - R: Exposure almost
	done IRQ enabled
	[2:2] – AUTOEXPMAX
	Enable IRQ when new calculated exposure is above configured max expo-
	sure
	0: DIS - W: Disable auto-exposure max IRQ - R: Auto-exposure max IRQ disabled
	1: EN - W: Enable auto-exposure max IRQ - R: Auto-exposure max IRQ enabled
	[3:3] – AUTOEXPMIN
	Enable IRQ when new calculated exposure is under configured min expo-
	sure
	0: DIS - W: Disable auto-exposure min IRQ - R:Auto-exposure min
	IRQ disabled
	1: EN - W: Enable auto-exposure min IRQ - R: Auto-exposure min
	IRQ enabled
	[4:4] – AUTOEXPOV
	Enable IRQ when new calculated exposure is larger than 16bit range
	0: DIS - W: Disable auto-exposure overflow IRQ - R: Auto-exposure
	overflow IRQ disabled
	1: EN - W: Enable auto-exposure overflow IRQ - R: Auto-exposure
	overflow IRQ enabled

#### 2.2.5.11 IRQFLG

IRQFLG	IRQ flag register
Address	0x0E
Reset value	0x00

Access	read-only
Fields	[0:0] – CPTDONE
	Capture done IRQ flag
	0: NFLG - R: Capture done IRQ flag has not been raised
	1: FLG - R: Capture done IRQ flag has been raised
	[1:1] – EXPAD
	Exposure almost done IRQ flag
	0: NFLG - R: Exposure almost done IRQ flag has not been raised
	1: FLG - R: Exposure almost done IRQ flag has been raised
	[2:2] – AUTOEXPMAX
	Auto-exposure above maximum value flag
	0: DIS - R: Auto-exposure max IRQ flag has not been raised
	1: EN - R: Auto-exposure max IRQ flag has been raised
	[3:3] – AUTOEXPMIN – Auto-exposure under minimum value flag
	0: DIS - R: Auto-exposure min IRQ flag has not been raised
	1: EN - R: Auto-exposure min IRQ flag has been raised
	[4:4] – AUTOEXPOV – Auto-exposure is larger than 16bit range flag
	0: DIS - R: Auto-exposure overflow IRQ flag has not been raised
	1: EN - R: Auto-exposure overflow IRQ flag has been raised

#### 2.2.5.12 IRQCLR

IRQCLR	IRQ clear register
Address	Ov0E
Address	0x0F
Reset value	0x00
Access	write-only
Fields	[0:0] – CPTDONE
	Clear capture done IRQ
	0: NONE - W: No effect
	1: CLR - W: Clear IRQ
	[1:1] – EXPAD
	Clear exposure almost done IRQ
	0: NONE - W: No effect
	1: CLR - W: Clear IRQ
	[2:2] – AUTOEXPMAX
	Clear auto-exposure above maximum value flag
	0: DIS - W: No effect
	1: EN - W: Clear IRQ
	[3:3] – AUTOEXPMIN
	Clear auto-exposure under minimum value flag
	0: DIS - W: No effect
	1: EN - W: Clear IRQ
	[4:4] – AUTOEXPOV
	Clear auto-exposure is larger than 16bit range flag
	0: DIS - W: No effect
	1: EN - W: Clear IRQ

## 2.2.5.13 ROI\_EN

ROI_EN	Range of interest enable register

Address	0x10
Reset value	0x00
Access	read-write
Fields	[0:0] – EN
	Range of interest enable field
	0: DIS - W: Disable range of interest - R: Range of interest disabled
	1: EN - W: Enable range of interest - R: Range of interest enabled

#### 2.2.5.14 ROI\_X\_START

ROI_X_START	Range of interest X start
Address	0x11
Reset value	0x00
Access	read-write
Fields	[4:0] - ROI_X_START
	Range of interest X start field. Must be between 0 and 19 included

#### 2.2.5.15 ROI\_X\_END

ROI_X_END	Range of interest X end
Address	0x12
Reset value	0x13
Access	read-write
Fields	[4:0] - ROI_X_END
	Range of interest X end field. Must be between 0 and 19 included

#### 2.2.5.16 ROI\_Y\_START

ROI_Y_START	Range of interest Y start
Address	0x13
Reset value	0x00
Access	read-write
Fields	[3:0] - ROI_Y_START
	Range of interest Y start field. Must be between 0 and 14 included

## 2.2.5.17 ROI\_Y\_END

ROI_Y_END	Range of interest Y end
Address	0x14
Reset value	0x0E
Access	read-write
Fields	[3:0] - ROI_Y_END
	Range of interest Y end field. Must be between 0 and 14 included

#### **2.2.5.18 RESOLUTION**

RESOLUTION	Frame resolution
Address	0x15
Reset value	0x00

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Access	read-write
Fields	[1:0] – RES
	Select the resolution for the output frame
	0: VGA - W: Select VGA resolution (640480p) - R: VGA resolution
	(640480p) selected
	1: QVGA - W: Select QVGA resolution (320240p) - R: QVGA resolu-
	tion (320240p) selected
	2: QQVGA - W: Select QQVGA resolution (160120p) - R: QQVGA
	resolution (160120p) selected

#### 2.2.5.19 LAGGREG

LAGGREG	Line aggregation register
Address	0x16
Reset value	0x00
Access	read-write
Fields	[2:0] - AGGREG Indicates how many pixels on the same line will be aggregated together  0: 1PIX - W: Disable aggregation - R: Aggregation disabled 1: 2PIX - W: Aggregate pixels together by 2 - R: Pixels will be aggregated together by 2 2: 4PIX - W: Aggregate pixels together by 4 - R: Pixels will be aggregated together by 4 3: 8PIX - W: Aggregate pixels together by 8 - R: Pixels will be aggregated together by 8 4: 16PIX - W: Aggregate pixels together by 16 - R: Pixels will be aggregated together by 16 5: 32PIX - W: Aggregate pixels together by 32 - R: Pixels will be aggregated together by 32

#### 2.2.5.20 EDGEMAP

EDGEMAP	Edge map register
Address	0x17
Reset value	0x00
Access	read-write
Fields	[0:0] - ENABLE
	Enable edge map using SOBEL algorithm
	0: DIS - W: Disable edge map - R: Edge map disabled
	1: EN - W: Enable edge map - R: Edge map enabled

## **2.2.5.21 EDGEMAP\_THR\_B0**

EDGEMAP_THR_B0	Edge map threshold LSB register
Address	0x18
Reset value	0x00
Access	read-write
Fields	[7:0] - THR
	LSB for the threshold value

#### **2.2.5.22 EDGEMAP\_THR\_B1**

EDGEMAP_THR_B1	Edge map threshold MSB register
Address	0x19
Reset value	0x00
Access	read-write
Fields	[0:0] - THR
	MSB for the threshold value

#### 2.2.5.23 FLIP

FLIP	Flip register
Address	0x1A
Reset value	0x00
Access	read-write
Fields	[0:0] - HORIZONTAL
	Enable horizontal flip of the picture
	0: DIS - W: Disable horizontal flip - R: Horizontal flip disabled
	1: EN - W: Enable horizontal flip - R: Horizontal flip enabled
	[1:1] - VERTICAL
	Enable vertical flip of the picture
	0: DIS - W: Disable vertical flip - R: Vertical flip disabled
	1: EN - W: Enable vertical flip - R: Vertical flip enabled

#### 2.2.5.24 AUTO EXPOSURE

AUTO_EXPOSURE	Auto exposure register (not applicable in this version).
Address	0x20
Reset value	0x00
Access	read-write
Fields	[0:0] - EN
	Not applicable in this version
	0: DIS - W: Disable auto-exposure - R: Auto-exposure disabled
	1: EN - W: Enable auto-exposure - R: Auto-exposure enabled

#### 2.2.5.25 AUTOEXPTRGT\_B0

AUTOEXPTRGT_B0	Auto exposure target LSB register
Address	0x21
Reset value	0x00
Access	read-write
Fields	[7:0] - TRGT
	LSB of target for mean pixel value in auto exposure mode

#### 2.2.5.26 AUTOEXPTRGT B1

AUTOEXPTRGT_B1	Auto exposure target MSB register
Address	0x22
Reset value	0x02

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Access	read-write
Fields	[1:0] - TRGT
	MSB of target for mean pixel value in auto exposure mode

#### **2.2.5.27 AUTOEXPMAX\_B0**

AUTOEXPMAX_B0	Auto exposure maximum value LSB register
Address	0x23
Reset value	0xFF
Access	read-write
Fields	[7:0] - MAX
	LSB of maximum exposure value in auto exposure mode

#### **2.2.5.28 AUTOEXPMAX\_B1**

AUTOEXPMAX_B1	Auto exposure maximum value MSB register
Address	0x24
Reset value	0xFF
Access	read-write
Fields	[7:0] - MAX
	MSB of maximum exposure value in auto exposure mode

#### **2.2.5.29 AUTOEXPMIN\_B0**

AUTOEXPMIN_B0	Auto exposure minimum value LSB register
Address	0x25
Reset value	0x00
Access	read-write
Fields	[7:0] - MIN
	LSB of minimum exposure value in auto exposure mode

## **2.2.5.30 AUTOEXPMIN\_B1**

AUTOEXPMIN_B1	Auto exposure minimum value MSB register
Address	0x26
Reset value	0x00
Access	read-write
Fields	[7:0] - MIN
	MSB of minimum exposure value in auto exposure mode

#### 2.2.5.31 HDR RSTHIGH B0

HDR_RSTHIGH_B0	HDR reset high LSB register (manual HDR)
Address	0x28
Reset value	0x7F
Access	read-write
Fields	[7:0] - HDR_RSTHIGH_B0
	LSB of the exposure count value when reset high is applied in manual HDR capture mode. It must differ from the RSTMID and RTSLOW

#### **2.2.5.32 HDR\_RSTHIGH\_B1**

HDR_RSTHIGH_B1	HDR reset high MSB register (manual HDR)
Address	0x29
Reset value	0x00
Access	read-write
Fields	[7:0] - HDR_RSTHIGH_B1
	MSB of the exposure count value when reset high is applied in manual
	HDR capture mode. It must differ from the RSTMID and RTSLOW

#### 2.2.5.33 HDR\_RSTMID\_B0

HDR_RSTMID_B0	HDR reset mid LSB register (manual HDR)
Address	0x2A
Reset value	0x07
Access	read-write
Fields	[7:0] - HDR_RSTMID_B0
	LSB of the exposure count value when reset mid is applied in manual
	HDR capture mode. It must differ from the RSTHIGH and RTSLOW

#### 2.2.5.34 HDR RSTMID B1

HDR_RSTMID_B1	HDR reset mid MSB register (manual HDR)
Address	0x2B
Reset value	0x00
Access	read-write
Fields	[7:0] - HDR_RSTMID_B1
	MSB of the exposure count value when reset mid is applied in manual
	HDR capture mode. It must differ from the RSTMID and RTSLOW

#### 2.2.5.35 HDR\_RSTLOW\_B0

HDR_RSTLOW_B0	HDR reset low LSB register (manual HDR)
Address	0x2C
Reset value	0x01
Access	read-write
Fields	[7:0] - HDR_RSTLOW_B0
	LSB of the exposure count value when reset low is applied in manual
	HDR capture mode. It must differ from the RSTMID and RTSLOW

#### 2.2.5.36 HDR\_RSTLOW\_B1

HDR_RSTLOW_B1	HDR reset low MSB register (manual HDR)
Address	0x2D
Reset value	0x00
Access	read-write
Fields	[7:0] - HDR_RSTLOW_B1

MSB of the exposure count value when reset low is applied in manual
HDR capture mode. It must differ from the RSTMID and RTSLOW

#### 2.2.5.37 ANALOG\_GAIN

ANALOG_GAIN	Analog gain
Address	0x30
Reset value	0x06
Access	read-write
Fields	[3:0] - GAIN
	Analog gain

#### 2.2.5.38 CCLK\_CAL

CCLK_CAL	CCLK calibration register
Address	0x31
Reset value	0x78
Access	read-write
Fields	[7:0] - CCLK_CAL
	Calibration for CCLK

## 2.2.5.39 MCLK\_DIV

MCLK_DIV	MCLK divider register
Address	0x32
Reset value	0x00
Access	read-write
Fields	[2:0] - DIV
	Divider for MCLK
	0: DIV1 - W: Select 6'b000001 div - R: 6'b000001 div selected
	1: DIV2 - W: Select 6'b000010 div - R: 6'b000010 div selected
	2: DIV4 - W: Select 6'b000100 div - R: 6'b000100 div selected
	3: DIV8 - W: Select 6'b001000 div - R: 6'b001000 div selected
	4: DIV16 - W: Select 6'b010000 div - R: 6'b010000 div selected
	5: DIV32 - W: Select 6'b100000 div - R: 6'b100000 div selected

## 2.2.5.40 CCLK\_DIV

CCLK_DIV	CCLK divider register
Address	0x33
Reset value	0x05
Access	read-write
Fields	[2:0] - DIV
	Divider for CCLK
	0: DIV1 - W: Select 6'b000001 div - R: 6'b000001 div selected
	1: DIV2 - W: Select 6'b000010 div - R: 6'b000010 div selected
	2: DIV4 - W: Select 6'b000100 div - R: 6'b000100 div selected
	3: DIV8 - W: Select 6'b001000 div - R: 6'b001000 div selected
	4: DIV16 - W: Select 6'b010000 div - R: 6'b010000 div selected

## 2.2.5.41 CCLK\_MUX

CCLK_MUX	CCLK MUX register
Address	0x34
Reset value	0x00
Access	read-write
Fields	[0:0] - SEL
	Select for CCLK
	0: CLKGEN - W: Select clock gen for CCLK - R: clock gen selected for
	CCLK
	1: CLKDIV - W: Select clock div for CLKDIV - R: clock div selected for
	CCLK

#### 2.2.5.42 CAL\_CLK\_BUFF\_B0

CAL_CLK_BUFF_B0	Calibration clock buffer LSBs register
Address	0x35
Reset value	0x00
Access	read-only
Fields	[7:0] - CAL_CLK_BUFF_B0
	Calibration clock buffer LSBs. This register is set when a capture is per-
	formed in CAL_CLK mode. It contains the number of CCLK cycles in a
	period of 46,875kHz (for a system clock of 24MHz). You need to wait
	for the CPT IRQ before reading this register. Reading this register be-
	fore the IRQ has been set can lead to non-predictable results

#### 2.2.5.43 CAL CLK BUFF B1

2.2.3.43 CAL_CLK_DOTT_DI	
CAL CLK BUFF B1	Calibration clock buffer MSBs register
Address	0x36
Reset value	0x00
Access	read-only
Fields	[7:0] - CAL_CLK_BUFF_B1
	Calibration clock buffer MSBs. This register is set when a capture is
	performed in CAL_CLK mode. It contains the number of CCLK cycles in
	a period of 46,875kHz (for a system clock of 24MHz). You need to wait
	for the CPT IRQ before reading this register. Reading this register be-
	fore the IRQ has been set can lead to non-predictable results

#### 2.2.5.44 CAL\_RAMP\_COUNT\_B0

CAL_RAMP_COUNT_B0	Calibration ramp count LSB register	
Address	0x37	
Reset value	0x00	
Access	read-only	
Fields	[7:0] - CAL_RAMP_COUNT	

Calibration ramp count LSB. This register is set when a capture is
performed in CAL_SO or CAL_DRS mode. It contains the sum of a
non-exposed column of pixels. You need to wait for the CPT IRQ
before reading this register. Reading this register before the IRQ
has been set can lead to non-predictable results

#### 2.2.5.45 CAL\_RAMP\_COUNT\_B1

CAL_RAMP_COUNT_B1	Calibration ramp count middle byte register
Address	0x38
Reset value	0x00
Access	read-only
Fields	[7:0] - CAL_RAMP_COUNT Calibration ramp count middle byte. This register is set when a capture is performed in CAL_SO or CAL_DRS mode. It contains the sum of a non-exposed column of pixels. You need to wait for the CPT IRQ before reading this register. Reading this register before the IRQ has been set can lead to non-predictable results

## 2.2.5.46 CAL\_RAMP\_COUNT\_B2

CAL_RAMP_COUNT_B2	Calibration ramp count MSB register
Address	0x39
Reset value	0x00
Access	read-only
Fields	[7:0] - CAL_RAMP_COUNT
	Calibration ramp count MSB. This register is set when a capture is
	performed in CAL_SO or CAL_DRS mode. It contains the sum of a
	non-exposed column of pixels. You need to wait for the CPT IRQ
	before reading this register. Reading this register before the IRQ
	has been set can lead to non-predictable results

## 2.2.5.47 IO DRIVE CAL

2.2.3.47 IO_DINIVE_CAL	
IO_DRIVE_CAL	IO drive calibration register
Address	0x3A
Reset value	0x01
Access	read-write
Fields	[0:0] - CAL
	IO drive calibration

## 2.2.5.48 ABB\_EN

ABB_EN	ABB enable register
Address	0x3B
Reset value	0x01
Access	read-write
Fields	[0:0] - EN
	ABB enable field

0: DIS - W: Disable ABB - R: ABB disabled
1: EN - W: Enable ABB - R: ABB enabled

#### 2.2.5.49 DPCORR

DPCORR	Dead pixel correction register
Address	0x40
Reset value	0x00
Access	read-write
Fields	[0:0] - EN
	Dead pixel correction enable field
	0: DIS - W: Disable dead pixel correction - R: Dead pixel correction
	disabled
	1: EN - W: Enable dead pixel correction - R: Dead pixel correction
	enabled

#### 2.2.5.50 DPO BO

DP0_B0	Dead pixel 0 address Byte0
Address	0x41
Reset value	0xFF
Access	read-write
Fields	[7:0] – COLLSB LSB column field

#### 2.2.5.51 DP0\_B1

DP0_B1	Dead pixel 0 address Byte1
Address	0x42
Reset value	0xFF
Access	read-write
Fields	[1:0] – COLMSB MSB column field
	[7:2] – ROWLSB LSB row field

## 2.2.5.52 DP0\_B2

DP0_B2	Dead pixel 0 address Byte2
Address	0x43
Reset value	0x07
Access	read-write
Fields	[2:0] - ROWMSB
	MSB row field

## 2.2.5.53 DP1\_B0

DP1_B0	Dead pixel 1 address Byte0
Address	0x44
Reset value	0xFF
Access	read-write
Fields	[7:0] - COLLSB

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LSB column field	
------------------	--

#### 2.2.5.54 DP1\_B1

DP1_B1	Dead pixel 1 address Byte1
Address	0x45
Reset value	0xFF
Access	read-write
Fields	[1:0] - COLMSB
	MSB column field
	[7:2] - ROWLSB
	LSB row field

#### 2.2.5.55 DP1\_B2

DP1_B2	Dead pixel 1 address Byte2
Address	0x46
Reset value	0x07
Access	read-write
Fields	[2:0] – ROWMSB MSB row field

#### 2.2.5.56 TEST

TEST	Test register
Address	0x7E
Reset value	0x00
Access	read-write
Fields	[7:0] – TEST
	Reserved to test read/write operations of the SPI

#### 2.2.5.57 **VERSION**

VERSION	Version register
Address	0x7F
Reset value	0x05
Access	read-only
Fields	[7:0] - VERSION
	Version field

## 2.2.6 Main electrical characteristics

Symbol	Definition	Condition	Min.	Тур.	Max.	Unit
V <sub>DDH</sub>	IO supply + core supply		1.62	1.8	1.98	٧
$V_{DDLD}$	Digital supply		0.81	0.9	0.99	V
V <sub>DDLA</sub>	Analog supply		0.81	0.9	0.99	V
Ivddh	Leakage current on VDDH	Deep sleep		0.047		μΑ

I <sub>VDDLD</sub>	Leakage current on VDDLD	Deep sleep		0.015		μА
I <sub>VDDLA</sub>	Leakage current on VDDLA	Deep sleep		0.011		μА
I <sub>VDDH</sub>	Leakage current on VDDH	Standby		0.06		μΑ
I <sub>VDDLD</sub>	Leakage current on VDDLD	Standby		0.007		μΑ
I <sub>VDDLA</sub>	Leakage current on VDDLA	Standby		4.59		μΑ
I <sub>VDDH</sub>	Operating current on VDDH	During cap- ture (DRS)		1.3		μΑ
I <sub>VDDLD</sub>	Operating current on VDDLD	During cap- ture (DRS)		625.41		μΑ
I <sub>VDDLA</sub>	Operating current on VDDLA	During cap- ture (DRS)		72.19		μΑ
Temperature	Temperature range		-40	25	85	°C
System frequency	Input clock frequency			12		MHz
Clock duty cycle				50		%
T <sub>rise</sub>	Input clock rise time			TBD		ps
T <sub>fall</sub>	Input clock fall time			TBD		ps
SPI clock frequency	SPI clock frequency			1		MHz

Table 4 Main electrical characteristics

#### 2.3 First evaluation results of the sensor

Prototypes will be available end of Q4 2020. Measurement results will be available mid Q1 2021. However, the test plan and the test software have already been developed. The idea behind the setup test is to be able to do anything via the computer.

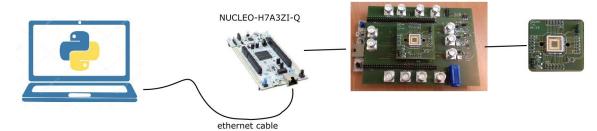


Figure 4 Test setup of the image sensor

A test software developed in Python will be used to send commands to the Nucleo board from ST Microelectronics. The test relies on a NUCLEO H743ZI2 with a STM32H743ZI2. This board features:

- An SPI interface to configure the imager
- 2MB of flash and 1.4MB of RAM
- DCMI interface with DMA connection to the RAM

- Ethernet interface
- Serial connection

The test software consists of a GUI with three parts. In the first part, all the registers of the imager can be either read/written individually or all at the same time. The second part has an image container and different capture buttons. The last part is dedicated to the communication with the Nucleo board. The messages coming from the Nucleo are also displayed in the user interface (see Figure 5).

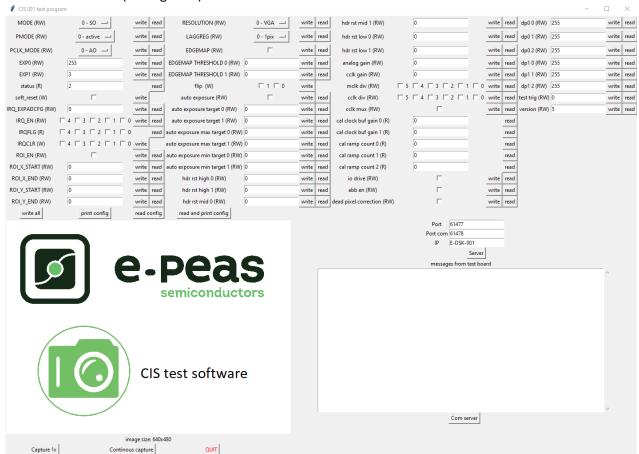
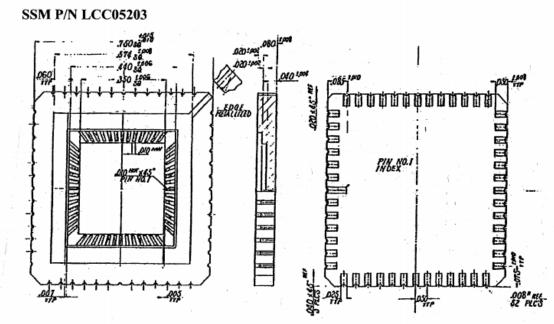


Figure 5 GUI of the python test software developed for the CISO01

#### 2.4 Prototype samples and final miniaturized samples

#### 2.4.1 Prototype samples: package drawing and pin assignment

The first prototype samples will be available in a CLCC52 package around November 2020. This is a leadless ceramic carrier (LCC). The packages have a glass window on top. Figure 6 shows the drawing of the package. Figure 7 depicts the pinout of the package.



#### NOTE

- L ALL EXPOSED METALLITED AREA SHALL BE GOLD PLATED.
- 2 SEAL RING FLATNESS DOJ
- 3. SEAL RING AND DIE ATTACH PAD ARE NOT GROUND TO A LEAD.

Figure 6 Drawing of the CLCC52 package used for the image sensor

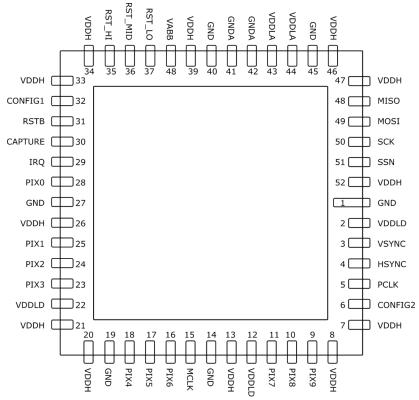


Figure 7 Pin assignment of the image sensor in the CLCC52 package

# 2.4.2 Final miniaturized samples for the ASSC

A packaging solution still has to be found for the miniaturized version.

#### 3 CO<sub>2</sub> sensor

#### 3.1 Objectives and requirements identified in WP1

#### 3.1.1 CO<sub>2</sub> SoA update

**Deliverable D1.1 - SoA and Gap analysis/recommendations on ESS features report** contains detailed information about a State-of-the-Art analysis of the CO<sub>2</sub> sensors available on the market. It includes in detail expected parameters about dimensions and power consumption. The AMANDA card requires a low profile (below 3mm) and low power components.

In D1.1, it was indicated that existing technologies do not fulfil the requirements of the AMANDA card:

- Devices with optical CO<sub>2</sub> detection method require an optical channel, which does not allow for sufficient miniaturisation
- Devices with electrochemical methods, even though promising from a miniaturisation point of view, require elevated temperatures to operate. That leads to relatively high energy consumption

In contrast to the above-mentioned devices, the IMEC sensor uses a technique of measurement that does not require optical channels, nor elevated temperatures. It has a unique technological potential to fit the project best.

The State-of-the-Art analysis needs to be updated (with respect to D1.1) due to a recent press releases by SENSIRION [8] and Infineon [9]. These communications describe very similar  $CO_2$  sensors with dimensions of ~10 x 10 x 6.5mm, less than the size of a sugar cube. This significant miniaturisation was made possible by using the heavy miniaturization of the method of photoacoustic sensing. However, the products are not yet commercially available and the power requirements are unknown. The thickness of the products does not fulfil the requirements of AMANDA, they might however prove to be interesting components for some use cases within AMANDA under the assumption that energy consumption is low enough.

#### 3.1.2 CO<sub>2</sub> sensor improvements within AMANDA

All components on an AMANDA device should fulfil the requirements concerning power consumption and dimensions. In the case of the IMEC CO<sub>2</sub> sensor we need to consider two components: the transducer (responding to changes in CO<sub>2</sub> concentration) and the readout (converting this response to a digital signal).

The CO<sub>2</sub> transducer is made of a silicon die of ~10 x 10mm with a thickness of ~1mm, with a thin layer of electrolyte deposited on top. These dimensions are a good fit for AMANDA and would fit on a card-like device. The impedance of these transducers is usually in the  $50 - 250 k\Omega$  range, meaning that currents are in the <  $10 \mu A$  range. This means the power consumption of the transducer during measurement should be sufficiently low.

Current IMEC readout modules have been miniaturized to fit within the AMANDA footprint. Power consumption can be tuned by using a duty cycle approach where the module is disconnected from power when not needed. It is to be expected however that due to the higher complexity of the CO<sub>2</sub> measurement, power consumption for this parameter will be significantly higher than for other parameters such as temperature or humidity. Technical details and specifications are given in the following Section.

#### 3.2 Sensor key specifications

The IMEC  $CO_2$  sensor is an in-house developed  $CO_2$  transducer combined with a dedicated electronic readout system. The block diagram in the Figure 8 shows basic components of the integrated sensor. The transducer consists of a silicon die with an interdigitated electrode, on top of which a layer of electrolyte is drop casted.  $CO_2$  interacts with the electrolyte, changing the electrical properties of the transducer. This change can be read out as a change of electric impedance by the readout system.

Changes of this analogue parameter need to be quantified and digitized. The measurements are done by an integrated circuit, embedded in the ADUCM355 microcontroller's analogue interface. The ADUMC355 is a State-of-the-Art IC which combines analogue circuitry with digital performance. Only by using an integrated solution, as proposed, can one achieve the miniaturization required in the AMANDA project.

As a result, a relatively low power, low profile, digital CO<sub>2</sub> sensor can be expected. Similar solutions for CO<sub>2</sub> measurement currently do not exist on the market.

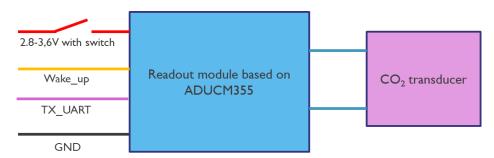


Figure 8 Block diagram of basic components of CO<sub>2</sub> sensor

In the next Sections, more detailed descriptions of the developed CO<sub>2</sub> transducer and readout can be found.

#### 3.2.1 CO<sub>2</sub> transducer

IMEC's CO<sub>2</sub> transducers consist of a thin layer of non-volatile electrolyte on a carrier surface having interdigitated electrodes. A very common variation are platinum electrodes on a silicon die, as these can be made and processed in higher volumes using standard wafer technology. Other materials such as glass as a carrier or gold electrodes are also well-known. The physical dimensions are determined by the design of the silicon wafers, in our case the dies had a size of ~10 x 10mm and a standard wafer thickness of 775 $\mu$ m. This is much smaller compared to commercially available devices and well within the specifications for AMANDA, although it should be noted that the die is merely a transducer which cannot operate without the readout circuit.

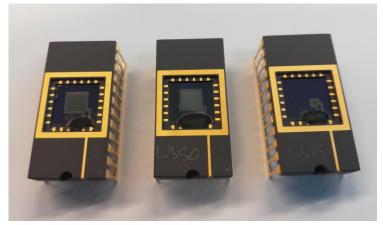


Figure 9 Typical examples of Pt on Si sensor dies with different electrode geometries

In order to achieve long sensor lifetime, all components of the transducer need to be stable. Often the electrolytes do not fulfil these requirements as many are based on aqueous solutions where evaporation leads to instability over time. IMEC's approach uses room-temperature liquid salts, so-called ionic liquids, as electrolytes. Being salts, these compounds exhibit

no measurable vapour pressure and therefore do not evaporate over time, even at elevated temperature or low pressure. Moreover, the ionic liquids used in this application show high thermal and (electro) chemical stability, making it possible to achieve sensor lifetimes in the range of several years. Thus, it is possible to fulfil the project requirements of 10 years of operation.

As  $CO_2$  is a highly stable molecule, an oxidative/reductive approach to sensing (similar to CO or  $NO_2$ ) is not possible. There is however a strong natural interaction of  $CO_2$  with ionic liquids, which can be observed by measuring the impedance of the electrolyte layer. Other parameters such as relative humidity and temperature will also influence impedance. However, these cross-sensitivities need to be quantified as their effects need to be eliminated from the result. Ionic liquid cannot stand standard soldering processes where temperature is elevated significantly above  $200^{\circ}C$  for several minutes. The ionic liquid needs to be placed on the sensing electrodes in a post soldering process. This requirement needs to be taken under account in AMANDA card production flow.

The interaction of  $CO_2$  with the electrolyte and the electrodes is quite specific, with only gases like  $SO_2$  or  $NO_2$  giving similar reactions. These gases are only present in minimal (up to low ppm) amounts compared to the 400ppm background concentration of  $CO_2$ , so this cross-sensitivity will not have a significant impact.

Current commercial NDIR-based devices show accuracies of  $\pm 30$ ppm with ranges up to 2000, 5000 or 10000ppm (1%). For most applications a relevant range of up to 2000ppm would be sufficient. Looking at general properties and the first data described in Section 3.4.3, specifications concerning lifetime and accuracy both seem feasible, making the ionic liquid based CO<sub>2</sub> sensor a good match for the AMANDA project.

#### 3.2.2 Readout electronics

#### 3.2.2.1 Implementation of CO<sub>2</sub> readout

Due to exposure to  $CO_2$  gas, the transducer will change its impedance. Measuring this change in impedance by using low power and low-profile electronics is a technical challenge. First, the parameter needs to be transformed to a voltage signal. The higher integration level of functional components simplifies miniaturization and makes it more suitable for the proposed AMANDA card applications described in **Deliverable D1.3 - Voice-of-the Customer completed**. The best performance can be achieved by developing a dedicated ASIC. However, this requires specific knowledge, tools and time however. Even though IMEC is technically able to do so, for newly developed sensors, it makes more sense to use off the shelf components for readout. Because of this, it was proposed that the novel  $CO_2$  transducer will be developed, and an off-the-shelf component-based readout system will be designed. A dedicated ASIC can be proposed for project continuation.

Before a dedicated readout circuit was available, the sensor response was measured using commercial and expensive laboratory potentiostats, e.g. the Bio-Logic SP-300. This approach is desirable for sensor characterisation as it gives excellent results, but miniaturization is needed for the final AMANDA card integration.

Reading of the transducer response is implemented by commercial electronic components. IC manufacturer Analogue Devices Inc. (ADI) has released several generations of components which are able to measure impedance. Early devices consisted of only an analogue interface with an ADC (AD5933) [10]. These were followed by a combined microcontroller/analogue interface with the ADUCM350 [11], which was succeeded by the 2019 (post-AMANDA kick off) chip ADUCM355 [12]. The ADUCM355 is an integrated low power solution which consists of a microcontroller with 26 MHz Arm Cortex-M3 processor and a sophisticated analogue interface for impedance measurement. The parts are placed on separated dies and encapsulated in one

package. One huge advantage of the IC is that it is provided as a 6 × 5mm electronic component in a 72-lead LGA package. It requires only few small passive electronic components for operation, making it a good match for the miniaturization required in the AMANDA project. The older ADUCM350 device was not able to measure 10Hz frequency directly. However, with the developed algorithms this could be achieved at the expense of computing power, thus electric energy. With the launch of the ADUCM355 [13] the specifications were significantly improved, also supporting direct 10Hz frequency measurements and a higher integration of peripherals. One of the aspects of integration is that oscillators are already integrated inside the ADUCM355. Table 5 shows estimated key parameters which could be achieved with ADUCM350 and ADUCM355. A detailed description of our readout module with ADUCM355 is presented in following Sections.

Key parameter	ADUCM350	ADUCM355
Current consumption [mA]	20	9
Required area for electronics [mm]	17 x 15	14 x 12
Execution time [ms]	500	500

Table 5 Comparison of readout circuit parameters

#### 3.2.2.2 AFE for CO<sub>2</sub> sensor

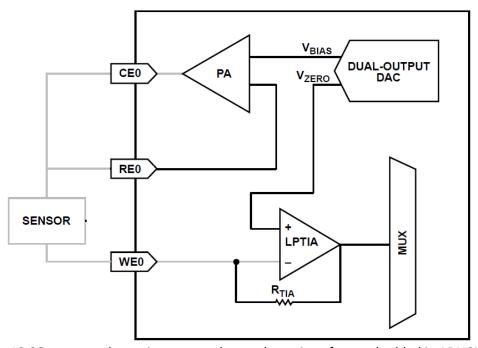


Figure 10 CO<sub>2</sub> sensor schematic connected to analogue interface embedded in ADUCM355

Figure 10 presents a simplified diagram of the integrated AFE of the ADUCM355 component. Measurements are performed by programming the DAC to generate a sinusoidal excitation. The signal is enforced by a Power Amplifier PA. The PA is configured as a voltage follower by shorting the CEO and REO pins. A strong sinusoidal excitation with an amplitude of 15mV and frequency of 10Hz is provided to the gas transducer, leading to a response that is directly

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measured as electric current by an LPTIA (Low Power Trans Impedance Amplifier). The operational amplifier in the TIA configuration converts the signal to a voltage. Then the analogue (voltage) signal is transferred via multiplexer MUX to the ADC to be digitalized.

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## 4 Capacitive sensor

# 4.1 Objectives and requirements identified in WP1

## 4.1.1 Conclusions from the SoA and Gap analyses

In the gap analysis documented in **Deliverable D1.1 - SoA and Gap analysis/recommendations on ESS features report** it has been concluded that the most important improvement of the capacitive sensor should concentrate on reducing the power consumption further, because the sensor is intended to be used as an always-powered with wake-up functionality. A power reduction directly translates to longer battery life of the ASSC in dark conditions where little or no energy can be harvested.

It was also concluded, that the existing MS8891 architecture should be used as a starting point for the AMANDA sensor development MS8892. Suggested improvements over the existing MS8891 included:

- Self-calibration feature to compensate manufacturing tolerances
- Auto-calibration feature to compensate slowly changing environmental conditions such as temperature, moisture or dirt assembling on the sensor
- Optimize EMC robustness while keeping the power consumption as is or reduce it even further
- Availability as chip-scale package with reflow-capable solder bump technology In the initial requirements **Deliverable D1.2 Initial System Requirements**, there was a further refinement of the requirements for the AMANDA sensor MS8892, as follows:
  - Only one sensor channel will be implemented, due to area and OTP memory limitations of the semi-custom array
  - Implementation of auto-calibration / auto-tracking of the switching threshold in COM-Pare mode
  - Possible reduction of power consumption in periodic COMPare mode (Op-mode-2) by reducing Idd idle with oscillator enabled
  - Improvement of noise immunity if required and if power consumption is not increasing
  - Providing the sensor in the smallest possible CSP package

#### 4.1.2 Definition of the role in the system

During the development of the architecture for the AMANDA ASSC, documented in **Deliverables D1.2** - **Initial system requirements specified, D1.6** - **Full system specification and BOM delivered,** and **D1.7** - **Architecture design of the AMANDA system delivered,** the role of the capacitive sensor in the system has been clarified and adapted. The capacitive sensor now has the function of the main wake-up source from the lowest power sleep mode, together with the RTC. It still also serves as a human interface device when the ASSC is in an active mode. The elements of the power management subsystem of the AMANDA ASSC are highlighted in Figure 11 below. These circuit parts are always powered as soon as there is some energy harvested and stored in the battery. The remainder of the system is completely powered off in the lowest power mode in order to save even the leakage current of the other components. The capacitive sensor (CAP TOUCH in Figure 11) and the RTC are the wake-up sources from this lowest power state. When a touch is detected or an RTC timer event happens, the power towards the MCU is enabled and the system is activated.

In order to extend the battery life time to its maximum, it is critical that this subsystem consumes as little energy as possible because it is always powered. Therefore, it was considered beneficial, to only have a single oscillator permanently running, instead of one in each of the wake-up sources (the capacitive sensor and the RTC). This led to the decision to add an external clock input to the capacitive sensor and use the oscillator of the RTC to trigger the periodic capacitive touch detections. With this feature, the power consumption of the capacitive touch

circuit could be reduced from ~750nA to less than 100nA while actively sensing at 2 scans per second.

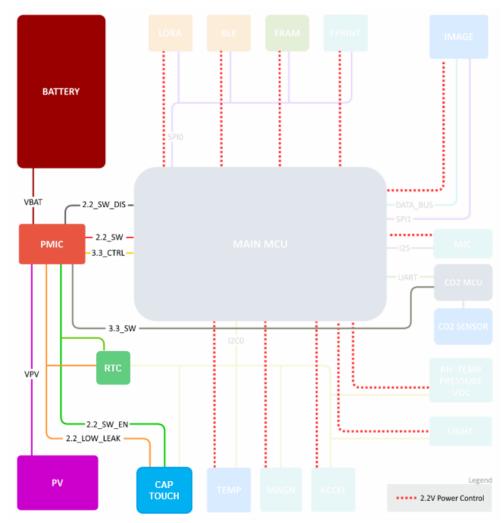


Figure 11 Power management subsystem of the AMANDA ASSC

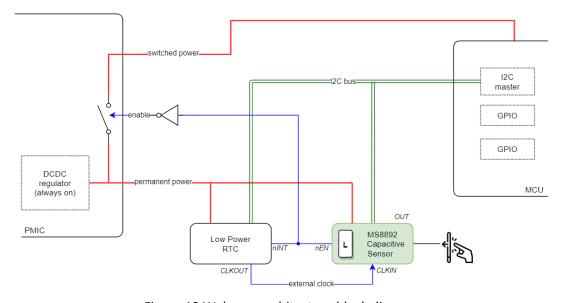


Figure 12 Wake-up architecture block diagram

Additional features defined and added to the capacitive touch sensor concern the sensor output. The sensor output can be connected to the RTC output in open-drain mode, and directly control the PMICs power state or an external PMOS power switch. A newly introduced internal latch allows the system power state to be registered. These features of the capacitive sensor make it an ideal companion to an external RTC also for similar applications outside the AMANDA project.

#### 4.1.3 Deviations from the initially planned specifications

As a result of the decisions taken, some of the objectives for the capacitive sensor initially stated in the AMANDA proposal have been adjusted:

- The power consumption target has been drastically reduced from ~750nA to below 100nA in the AMANDA system
- Additional logic functionality supporting the role as a system wake-up (power ON/OFF) device has been added
- As a trade-off, the planned automatic detection of slow capacitance changes (autocalibration) has been dropped and is replaced with an automatic compensation of manufacturing tolerances by providing a relative switching threshold setting<sup>1</sup>

In summary, the specification of the capacitive sensor has been refocused according to the requirements of AMANDA, while maintaining its sensing performance. The suitability of the device for use in energy harvesting IoT devices, wearables, and other ultra-low power applications has been further improved.

# 4.2 Sensor key specifications

#### 4.2.1 General description and main features

The integrated circuit MS8892 is an ultra-low power capacitive sensor specially designed for human body detection and as wake-up source for ultra-low power systems. It offers two operating modes: meter mode or switch mode. In switch mode the sensor capacitance is compared with the internal reference capacitance. The capacitance threshold can be set absolutely or relative to a baseline value, which is automatically determined and therefore includes fabrication and material tolerances. The comparator output is available at a circuit pin in switch mode or can be read via the I<sup>2</sup>C serial interface. The MS8892 can also be operated in meter mode where the absolute capacitance value of the sensor is measured. The MS8892 can optionally be operated with a latching output. In this configuration it can be used as a wake-up device and directly control a power-management IC (PMIC) or a PMOS type powerswitch for achieving the lowest possible power consumption for ultra-low power systems. An external clock input allows the power consumption of the MS8892 to be further minimized. This saves system power when a clock is already available from a real time clock (RTC) or nanotimer. The configuration of the various options is performed via the I<sup>2</sup>C serial interface. All settings can be programmed into the one-time-programmable (OTP) memory. When the options are programmed into the OTP, the MS8892 can be operated as a stand-alone solution without interfacing to an MCU.

The main features of the MS8892 are:

- Capacitive sensor with direct digital output
- Operation in meter mode (capacitance measurement) or switch mode (capacitance change detection)

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<sup>&</sup>lt;sup>1</sup> Adjustment of the switching threshold due to slowly changing sensor capacitance can still be achieved with the microcontroller (firmware) by triggering periodic baseline capacitance measurements.

- Average current for 2 measurements/s in switch mode typ. 65nA (no noise filter) with external clock source
- Average current for 2 measurements/s in switch mode typ. 725nA (no noise filter) with internal clock source
- Idle current typ. 50nA
- Latching output to directly control power state of a PMIC or a PMOS power switch
- Capacitance meter with a measuring range covering 0.2 to 1.0pF with a resolution of 8 hits
- Individually programmable threshold capacitance in switch mode
- Automatically adjusted switching threshold in switch mode with a programmable threshold step size
- Programmable measuring interval in switch mode
- Programmable noise filter in switch mode
- Comparator output at pin OUT in switch mode
- Programmable polarity of comparator output
- CMOS or open-drain output driver
- Internal switchable pull-up resistor in open-drain configuration to avoid static current in pull-up
- I<sup>2</sup>C serial interface available at pins SDA and SCL
- I<sup>2</sup>C address pin allowing operation of two MS8892 on a single bus
- No external components needed
- Sensor capacitance can be realized with conductive tracks on PCB or casing
- Voltage operating range 1.8 to 4.5V
- Temperature operating range -40 to 85°C
- Available in CSP12 1.52x1.03mm

#### 4.2.2 Pin description

Pin QFN	Pin CSP	Symbol	Туре	Description
1	2	VDD	supply	Positive supply voltage
2	3	A0	digital input	User-defined I <sup>2</sup> C sub-address bit 0, connect to VSS or VDD
3	4	TRIGGER	digital input	External trigger to start measurement in switch mode, connect to MCU, VDD or VSS, depending on chosen operating mode.  TRIGGER is also used for applying the programming voltage during programming of the OTP memory.
4	5	VSS	supply	Negative supply voltage
5				Not connected; pin can be left open
6	6	SA	digital output	Sensor electrode, driver signal
7				Not connected; pin can be left open
8	7	OUT	digital output	Switch state output, CMOS push-pull or open- drain with integrated pull-up resistor
9	8	INIT	digital input	(Re)initialize the baseline capacitance value in relative threshold mode

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				Reset the output state in latching mode
				Connect to VSS if not used in the application
10	9	RSTN	digital input	Reset input, low active, internal pull-up
11	10	CLKIN	digital input	External clock input
12	11	SDA	digital I/O	I <sup>2</sup> C-bus serial bidirectional data line; open-drain
13	12	SCL	digital input	I <sup>2</sup> C-bus serial clock input
14				Not connected; pin can be left open
15	1	SB	analog input	Sensor electrode, input signal
16				Not connected; pin can be left open

Table 6 MS8892 pin description

#### Notes:

- 1. SB is internally switched to VDD over an  $8k\Omega$  resistor when the measurement is inactive
- 2. The inputs TRIGGER, INIT, CLKIN, A0 must be connected to valid logic levels in the application
- 3. The input RSTN can be left floating or connected to a capacitor to VSS
- 4. The QFN package is an optional package option, which will only be available on request by customers

## 4.2.3 Typical applications

The following diagrams illustrate some of the typical application configurations of the MS8892.

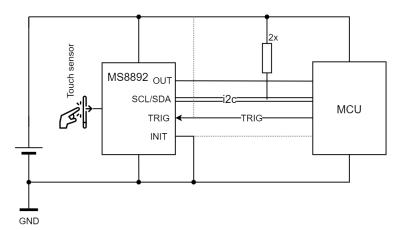


Figure 13 Normal touch or human body detector, MCU controlled, all types of measurements supported

#### Notes:

- Not all pins of the MS8892 are shown for reasons of simplicity of the figure, therefore:
- Pin A0 is supposed to be connected to either GND or VDD
- Pin RSTN can be left open or connected to a capacitor
- Pin CLKIN can be driven by an RTC as clock source, otherwise it should be connected to GND

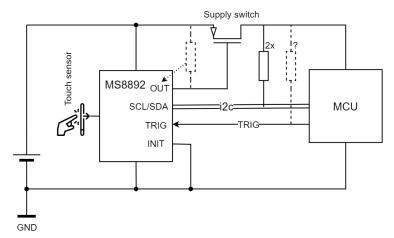


Figure 14 System power controller, MCU controlled, configuration from MCU or OTP, all types of measurement possible

#### Notes:

- The pull-up resistor shown with dashed lines at the OUT pin is integrated in the MS8892 and must not be placed externally
- The pull-up resistor attached to the TRIG signal is optional, and only needed if the MCU pin is configured with an open-drain output

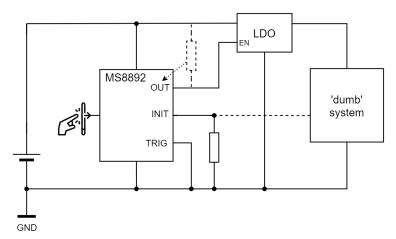


Figure 15 System power controller, stand-alone powering a 'dumb' system, configuration from OTP, with periodic compare measurements enabled

#### Notes:

 The pull-up resistor shown with dashed lines at the OUT pin is integrated in the MS8892 and must not be placed externally

#### 4.2.4 Block diagram and basic operation

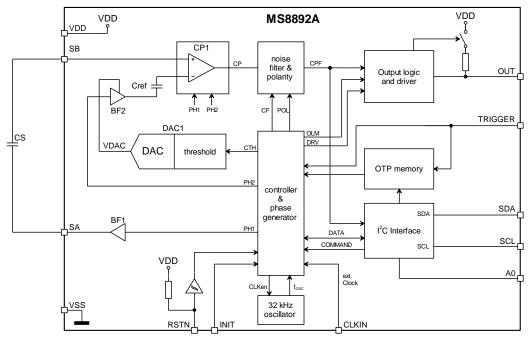


Figure 16 MS8892 top level block diagram

Figure 16 shows the block diagram of the circuit MS8892. The circuit has one capacitive sensor channel CS, consisting of sensor output SA and sensor input SB. The sensor capacitance is measured by comparing the charge transferred at the sensor input with a reference charge defined by Cref and the voltage VDAC. VDAC is the output of the digital-to-analog converter DAC1. The equilibrium, where both charges are equal is defined by the following equation.

$$V_{DD} \cdot CS = VDAC \cdot Cref$$

The MS8892 can be operated in meter mode or switch mode. In meter mode, the sensor capacitance CS is measured and converted to an 8-bit digital value which represents the absolute sensor capacitance. The measured value is read out via the I<sup>2</sup>C serial interface.

In switch mode the charge transferred from SA to the SB sensor input, which linearly depends on the sensor capacitance, is compared with a reference charge defined by Cref and VDAC. If the sensor capacitance drops below or rises above the threshold capacitance value  $C_{TH}$  is detected by the comparator CP1 and indicated by a change of the signal CP from logical '0' to logical '1'. Noise suppression is done with a programmable noise filter. The noise filter has three levels (no, low and high filter). The signal CPF is the sensor output after the noise filter and is available at the output OUT. The polarity of the sensor output can be set by the bit POL in register OPT2:

- POL = '0': OUT is logical '1' if C<sub>S</sub> is smaller than C<sub>TH</sub>
- POL = '1': OUT is logical '1' if C<sub>S</sub> is larger than C<sub>TH</sub>

The state of the switch mode output signal CPF can be read via the I<sup>2</sup>C serial interface. The external reset pin RSTN allows a reset from an attached controller or a watchdog circuit. Additionally, the reset duration can be extended in applications where noise or instability of the rising power-supply require a longer reset. The RSTN pin is internally connected with a pull-up resistor to VDD and the delay time can be defined by choosing the value of an externally connected capacitor CR to VSS.

The following sub-Sections describe the most important functionalities of the device. The full description is documented in the MS8892 datasheet [2], available from the Microdul website.

# 4.2.4.1 Measuring sequence in switch mode

In switch mode the capacitance of the sensor is compared with a capacitance threshold. A measurement in switch mode is either started with a single trigger (over input pin TRIGGER or by the I<sup>2</sup>C serial command COMP) or executed periodically.

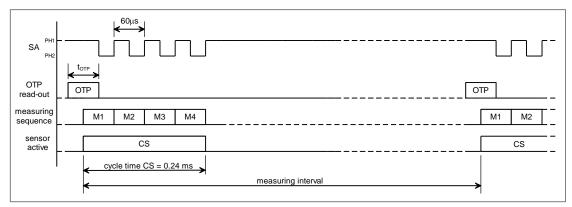


Figure 17 Example timing of measuring sequence in switch mode if noise filter is low (NoF = '0', CF = '0')

#### 4.2.4.2 Measuring sequence in meter mode

The meter mode is used to measure the absolute sensor capacitance of CS. The meter mode is started by sending the command MCS to the MS8892.

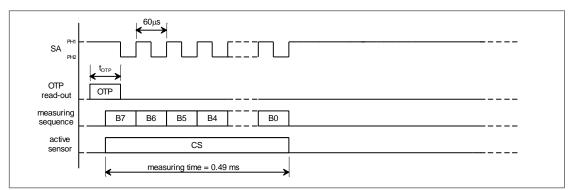


Figure 18 Timing of measuring sequence in meter mode

#### 4.2.4.3 External clock input, measuring interval generation

The MS8892 supports two clock sources selectable by the option CLKS[1:0] in register OPT1. The integrated oscillator is used as the main clock source, always controlling the measuring sequences. The oscillator runs nominally at  $f_{OSC} = 32.8 \text{kHz}$ .

If option CLKS[1] = '0' the internal oscillator runs continuously and controls the measuring interval defined with the parameter MI. If option CLKS[1] = '1' the external clock input on pin CLKIN is selected to control the measuring intervals defined in MI. In this case, the internal oscillator is powered down even in the periodic measurement modes, and is only started to perform the actual measuring sequences.

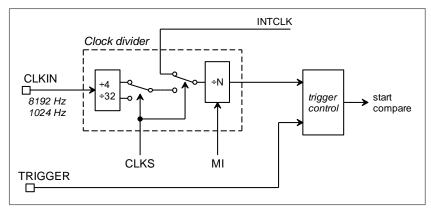


Figure 19 External clock input and generation of measuring interval

#### 4.2.4.4 Noise filtering, polarity selection and measurement duration

The output CP of the comparator is input to the polarity selection and the digital noise filter.

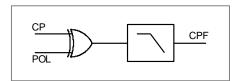


Figure 20 Polarity selection and digital noise filter

In normal situations, a touch of the sensor reduces the measured capacitance, and if the value falls below the threshold, the signal CP will rise. Option POL allows inversion of the polarity of the output signal.

In the filter, three different levels of noise suppression can be selected:

- No noise filter NoF = high
- Noise suppression CF = low: 4 measurements are performed per measurement phase, and the output changes if at least 3 of the 4 measurements are equal
- Noise suppression CF = high: 16 measurements are performed per measurement phase, and the output changes if at least 12 of the 16 measurements are equal

Filter setting	NoF	CF	Measurements	Min number of detections	Measurement duration
No filter	1	-	1	1	0.06ms
Low	0	0	4	3	0.24ms
High	0	1	16	12	0.98ms

Table 7 Noise filtering parameters

The filter setting determines the over-all measurement duration and therefore has an influence on the average power consumption.

## 4.2.4.5 Output logic, latching and driver

The output driver mode can be CMOS (output is driven active low or active high) or opendrain (output is driven active low only; high level must be achieved by the internal or an additional external pull-up resistor). In open-drain driver mode, option PUE enables or disables the internal pull-up resistor on pin OUT. If the pull-up resistor is enabled and OUT is driven to a low level, the resistor gets disconnected from OUT with the switch P2 in order to avoid static power dissipation.

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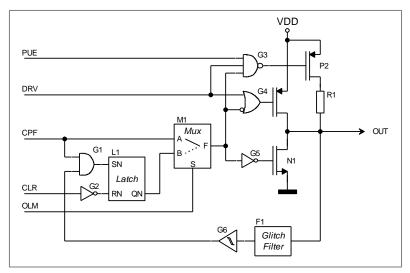


Figure 21 Output latch and drivers with integrated switched pull-up resistor

Option OLM defines the latching mode of the output stage. If the latching mode is enabled, each activation of the sensor is stored in the latch and the output will keep its state even when the sensor is de-activated again. Only active-low signals are stored in the latch. In open-drain mode, an external circuit can also pull the signal OUT low. If latching mode is enabled, this low state will also be stored in the latch, and OUT will remain driven low until the latch is cleared again.

Output driver mode and state	OLM	DRV	CPF	OUT
Direct output (not latching), CMOS push-pull		0	0	0
driver	0	O	1	1
Direct output (not latching), open-drain	U	1	0	0
driver			1	pulled-up
		0	0	0
Latching enabled, CMOS push-pull driver			1	0 (latch set) 1 (latch cleared)
	1		0	0
Latching enabled, open-drain driver		1	1	0 (latch set) pulled-up (latch cleared)

Table 8 Logic behaviour of the output stage

Note: In the open drain configurations (DRV = '1') it is assumed, that the internal pull-up resistor is enabled (PUE = '1'), or that an external pull-up resistor is attached to OUT.

#### 4.2.5 I<sup>2</sup>C Interface and register description

The MS8892 has a slave receiver/transmitter I<sup>2</sup>C serial interface for chip configuration, OTP programming, and readout of measurement results and internal states.

Bit	A6	A5	A4	А3	A2	A1	A0
Value	0	1	0	0	1	0	Α0

Table 9 MS8892 I<sup>2</sup>C address definition

The IC supports two 7-bit slave addresses, which are defined as:

- 0x24 if pin A0 is connected to VSS
- 0x25 if pin A0 is connected to VDD

## 4.2.5.1 I<sup>2</sup>C command table

Command byte value	Symbol	Function	Transfer type
00h	MCS	Measure CS	Command
01h	RCS	Read CS (register CVAL)	Read 1 byte
02h	COMP	Compare (switch mode)	Command
03h	RRES	Read comparison results (register RES)	Read 1 byte
04h	LCLR	Clear output latch	Command
05h	WTH	Write register RTH	Write 1 byte
06h	RTH	Read register RTH	Read 1 byte
07h	WOPT1	Write register OPT1	Write 1 byte
08h	ROPT1	Read register OPT1	Read 1 byte
09h	WOPT2	Write register OPT2	Write 1 byte
0Ah	ROPT2	Read register OPT2	Read 1 byte
0Bh	PTH	Program register RTH to OTP memory	Command
0Ch	POPT1	Program register OPT1 to OTP memory	Command
0Dh	POPT2	Program register OPT2 to OTP memory	Command

Table 10 MS8892 I<sup>2</sup>C command table

#### 4.2.5.2 Register descriptions

Habita Habita								
	Bit(s)	Symbol	Function	Reset value				
	7:0	CVAL[7:0]	Capacitance value of sensor CS (lower 8 bits B7B0). The value is binary coded. The LSB value is defined by the unit capacitance CU. This value serves also as the baseline value for the threshold in the automatic threshold setting mode.	,0000 0000,				

Table 11 Description of register CVAL – capacitance value of sensor CS

The RTH register has two interpretations. If the MS8892 is configured for a fixed absolute threshold (THM = '0' in register OPT2), then RTH contains the 8 bits FTH[7:0] of the fixed threshold capacitance as shown in Table 12. When the relative threshold mode is enabled (THM = '1' in register OPT2), then RTH contains the threshold step polarity bit (STP) and the 7-bit relative threshold step height (CSTEP) as shown in Table 13.

Bit(s)	Symbol	Function	Reset value
7:0	FTH[7:0]	Absolute threshold capacitance value for sensor CS in switch mode (lower 8 bits). The value is binary coded.	'0000 0000'
		The LSB value is defined by the unit capacitor CU.	

Table 12 Description of RTH (THM = '0') – threshold capacitance for sensor CS

Bit(s)	Symbol	Value	Function	Reset value
7	STP	'0' '1'	Relative threshold step polarity: negative threshold step positive threshold step	'0'
6:0	CSTEP[6:0]		Relative threshold step height. The value is binary coded. The LSB value is defined by the unit capacitor CU.  This value is added/subtracted to/from the threshold baseline value in CVAL to determine the switching threshold in relative threshold mode.	'000 0000'

Table 13 Description of RTH (THM = '1') – threshold step height

Bit(s)	Symbol	Value	Function	Reset value
7:6	n/a	n/a	n/a	n/a
5:4	CLKS[1:0]		Clock source selection:	'00'
		<b>'</b> 0-'	- internal oscillator (32kHz)	
		'10'	- external clock input, 1024Hz	
		'11'	- external clock input, 8192Hz	
3:2	MI[1:0]		Measuring interval:	'00'
		'00'	- single trigger	
		'01'	- periodic, 32 measurements per second	
		'10'	- periodic, 8 measurements per second	
		'11'	- periodic, 2 measurements per second	
1	NoF	<b>'</b> 0'	Noise filter switched on	'0'
		'1'	Noise filter switched off	
0	CF		Noise suppression:	'0'
		'0'	low (3/4 detections)	
		'1'	high (12/16 detections)	
			Note: Bit NoF overrules this setting	

Table 14 Description of OPT1 – options register 1

Bit(s)	Symbol	Value	Function	Reset value
7	n/a	n/a	n/a	n/a
6	THM		Absolute / relative threshold mode:	'0'
		'0'	absolute threshold mode	

		'1'	relative threshold mode	
5	PUE		Enable for internal pull-up resistor on OUT pin:	'0'
		'0'	Internal pull-up disabled	
		'1'	Internal pull-up enabled if in open-drain configuration (DRV = '1')	
4	OLM		Output latching mode	'0'
		'0'	Direct output mode, not latching	
		'1'	Latching output mode	
3	POL		Output polarity selection:	'0'
		'0'	not inverted, OUT is high if C <sub>s</sub> < C <sub>TH</sub>	
		'1'	inverted, OUT is high if C <sub>S</sub> > C <sub>TH</sub>	
2	DRV	'0'	CMOS output driver (OUT)	'0'
		'1'	Open-drain output driver (OUT)	
1	INT		Interrupt over I <sup>2</sup> C bus:	<b>'0'</b>
		'0'	Interrupt mode disabled	
		'1'	Interrupt if CPF state changes	
0	RAM		Source of configuration:	'0'
		'0'	ROM mode: RTH, OPT1, OPT2 are overwrit-	
			ten by corresponding OTP memory registers	
			prior to measurement	
		'1'	RAM mode: RTH, OPT1, OPT2 are never	
			overwritten prior to measurement	
			Note: The RAM bit is not written to or read	
			from OTP	

Table 15 Description of OPT2 – options register 2

Bit(s)	Symbol	Value	Function	Reset value
7:4	n/a		n/a	n/a
3	ERR	'0' '1'	Relative threshold calculation error state: Valid threshold calculation result Overflow (positive threshold step) or underflow (negative threshold step) has occurred in threshold calculation	<b>'</b> 0'
2	LATS	'0' '1'	Latching trigger source (when LAS = '1'): Output latching triggered internally by touch event Output latching triggered externally by pulling OUT low	'0'
1	LAS	'0' '1'	Output latching state: Output latch clear Output latch activated, OUT pulled active low	'0'

			Note: Output latching mode is only enabled when DRV = '1' and OLM = '1'. Otherwise LAS = '0'	
0	CPF	'0' '1'	Comparison result sensor CS: $C_S > C_{TH}$ (POL = '0') $C_S < C_{TH}$ (POL = '0') Note: The output value is inverted with POL = '1'	<b>'</b> 0'

Table 16 Description of RES – comparison result & latching state

# 4.2.6 DC and AC characteristics

Conditions:  $V_{DD}$  = 3V, Tamb = 25°C, if not stated otherwise

Symbol	Parameter	Min	Тур	Max	Unit
V <sub>DD</sub>	Positive supply voltage	1.8		4.5	V
I <sub>DD,INT</sub>	Idle state, oscillator disabled		50		nA
(supply current	Idle state, oscillator enabled, MI = periodic		720		nA
internal	Active current during measurement		11		μΑ
osc only)	Average current (switch mode), 2 measurements/s, CF = low		735		nA
	Average current (switch mode), 32 measurements/s, NoF = '1'		800		nA
	Average current (switch mode), 32 measurements/s, CF = low		860		nA
	Average current (switch mode), 32 measurements/s, CF = high		1.1		μА
I <sub>DD,EXT</sub> (supply	Idle state, oscillator disabled, f <sub>CLKIN</sub> = 8.192 kHz		tbd	100	nA
current external	Idle state, oscillator disabled, f <sub>CLKIN</sub> = 1.024 kHz		tbd	100	nA
osc used)	Average current (switch mode), 2 measurements/s, CF = low, f <sub>CLKIN</sub> = 8.192 kHz		tbd	100	nA
	Average current (switch mode), 2 measurements/s, CF = low, f <sub>CLKIN</sub> = 8.192 kHz		tbd	100	nA
	Average current (switch mode), 32 measurements/s, CF = low, f <sub>CLKIN</sub> = 1.024 kHz		tbd	100	nA
	Average current (switch mode), 32 measurements/s, CF = low, f <sub>CLKIN</sub> = 1.024 kHz		tbd	100	nA
CS <sub>typ</sub>	Typical range of sensor capacitance	200		1000	fF
CU	ADC resolution	2.95	3.1	3.25	fF
$V_{PROG}$	OTP programing voltage	9.9	10.0	10.1	V

R <sub>RSTN</sub>	Pull-up resistor on RSTN		153		kΩ
l <sub>OUT</sub>	Output current	-5		5	mA
R <sub>OUT</sub>	Switchable pull-up resistor on OUT		175		kΩ
T <sub>amb</sub>	Operating temperature range	-40	25	85	°C

Table 17 Selected MS8892 DC characteristics

Conditions:  $V_{DD} = 3V$ , Tamb = 25°C, if not stated otherwise

Symbol	Parameter	Min	Тур	Max	Unit
fosc	Oscillator frequency	30	32.8	35.6	kHz
t <sub>meas:sw</sub>	Compare measure time, NoF = '1'		0.06		ms
	Compare measure time, NoF = CF = '0'		0.24		ms
	Compare measure time, NoF = '0', CF = '1'		0.98		ms
t <sub>meas:meter</sub>	Capacitance measure time (meter)		0.49		ms
f <sub>MI</sub>	Measurement rate, MI[2:0] = '01'		32		Hz
	Measurement rate, MI[2:0] = '10'		8		Hz
	Measurement rate, MI[2:0] = '11'		2		Hz
f <sub>CLKIN</sub>	Ext clock frequency, CLKS[1:0] = '10'		1024		Hz
	Ext clock frequency, CLKS[1:0] = '11'		8192		Hz
t <sub>OTP</sub>	OTP read-out time		0.06		ms
t <sub>TRG</sub>	External single trigger	1	50	100	μs
t <sub>BLM</sub>	Baseline measurement trigger pulse width (pos. pulse on INIT)	1	50	100	μs
t <sub>LCLR</sub>	Delay of latch clearing (after setting INIT to '1')			2	ms
t <sub>RSTN</sub>	Reset pulse width, C <sub>RSTN</sub> = 1 nF		175		μs
	Reset pulse width, C <sub>RSTN</sub> = 100 nF		17.5		ms

Table 18 Selected MS8892 AC characteristics

# 4.3 First evaluation results of the sensor

## 4.3.1 Planning

First packaged prototype samples will be available in the second half of August 2020 (M20). First evaluation results are expected by the end of M20. The full evaluation is planned in the following months.

Event	Planned for	Comments
Wafer delivery	03.08.20	The wafers have arrived on the 31.07.20, earlier than planned.
Wafer grind and saw	19.08.20	1 wafer will be ground to 200 um thickness and sawn for prototype packaging and later used for QFN-16 samples.

Prototype package assembly	25.08.20	Die and wire bonding of the devices into the SOIC-16 package at Microdul
First quick evaluation	31.08.20	A first quick evaluation based on simple lab hardware is planned before the end of M20
Complete evaluation	31.10.20	The complete evaluation on dedicated lab hardware is planned for the end of M22

Table 19 Sample production & evaluation planning of the MS8892

#### 4.3.2 First quick evaluation

A first quick evaluation will be based on a simple hardware & software setup:

- National Instruments PXI system
- GUI programmed in Labview
  - Labview VI to configure the MS8892, trigger measurements, and read out capacitance values
  - Labview controls only the I<sup>2</sup>C communication
- Oscilloscope to observe the output OUT and other signals
- Supply current measurement in the PM2 power supply with 0.1uA accuracy

The Labview VI from the evaluation of the predecessor MS8891 will be adapted for this first functionality test.

This first evaluation will show the basic functionality of capacitance sensing and switching. Most essential functionality can be checked in this setup.

#### 4.3.3 Full sensor and sub-system evaluation

For the complete sensor and sub-system evaluation, a new evaluation setup will be designed with the following main characteristics & measuring possibilities:

- Control from NI PXI, including a parametrized supply voltage, and pulse generation on TRIG and INIT signals
- Flexible sensor input connectivity:
  - o Realistic touch sensor for manual touch operation
  - Variable voltage pulse source, for measuring the capacitance measurement range & linearity
- Placement option for the RV-3028-C7 RTC to supply the external clock to the MS8892 and to connect the outputs of the two circuits together (emulation of the AMANDA wake-up Section)
- P-MOS switch connected to the output signal (OUT pin), controlling a LED to indicate the output / latching state
- Possibility to accurately measure power consumption in the AMANDA system configuration including the RTC

#### 4.3.4 Evaluation results

The finished prototype samples have just been received at the date of the deadline for this document. Images of the samples are shown in Figure 24 and Figure 25 below.

The evaluation results of the capacitive sensor will be published in a different Deliverable, either in D2.5 - Finalised Prototypes Report or in D6.2 - Characterisation/test reports of individual components in lab environment.

# 4.4 Prototype samples and final miniaturized samples

## 4.4.1 Prototype samples

The MS8892 capacitive sensor prototype is delivered in a JEDEC compliant narrow SOIC-16 package [14] for integration in the unconstrained AMANDA platform. This package enables a fast-track assembly of the first untested silicon dies in-house at Microdul. Additionally, the package is suitable for mounting in a standard socket for electrical and functional evaluation of the ICs. In this way existing lab hardware can readily be reused.

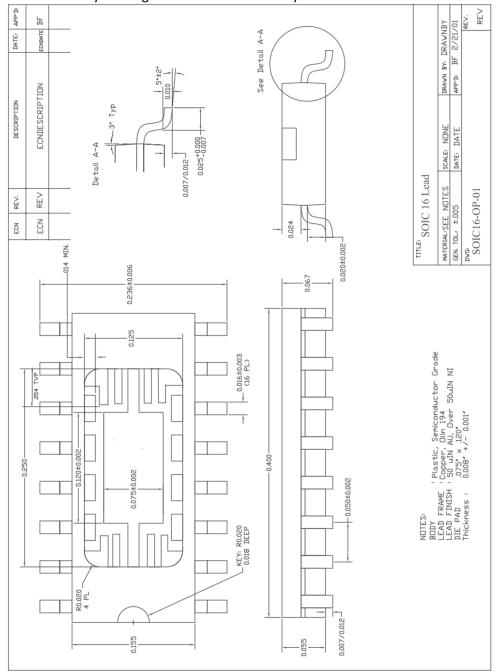


Figure 22 Physical dimensions of SOIC-16 open-top prototype package for MS8892

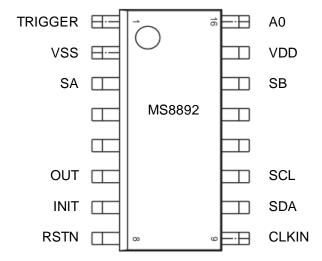


Figure 23 Pin assignment of MS8892 in SOIC-16 prototype package

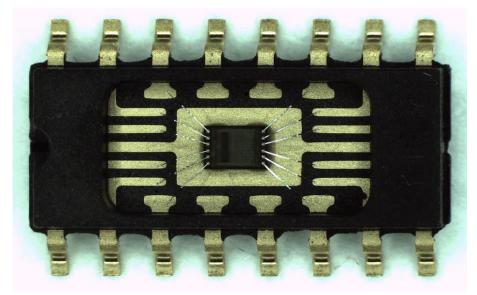


Figure 24 SOIC-16 prototype package assembled with MS8892

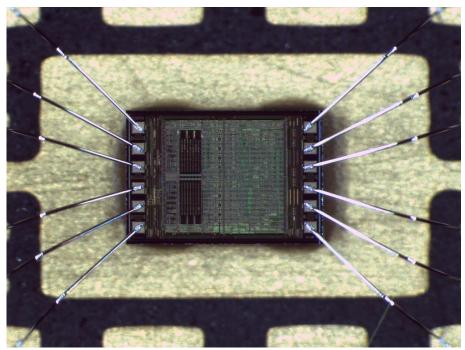


Figure 25 MS8892 chip bonded into the prototype package

# 4.4.2 Final miniaturized samples for the ASSC

# 4.4.2.1 CSP specification

Parameter	Value
CSP X	1520μm
CSP Y	1030μm
CSP Z	637µm
Nr. of I/Os	12
Min. Bump pitch	355µm
Bump height	100μm
Bump size	172μm
Bump material	Sn/Ag

Name	Pad	Ball coo	ordinate
		Xμm	Yμm
SB	1	74.40	-27.76
VDD	2	444.40	-32.76
A0	3	74.40	-334.76
TRIGGER	4	444.40	-387.76
VSS	5	444.40	-742.76
SA	6	74.40	-749.76
OUT	7	1264.40	-749.76
INIT	8	819.40	-742.76
RSTN	9	894.40	-387.76
CLKIN	10	1264.40	-334.76
SDA	11	894.40	-32.76
SCL	12	1264.40	-27.76

Table 20 CSP specification and solder ball coordinates of MS8892

## Notes on Table 20:

- Solder ball co-ordinates are from the centre of the ball
- Values for CSP X and CSP Y are after sawing
- CSP Z includes the bump height (over-all height)
- Coordinates are given relative to ball 1

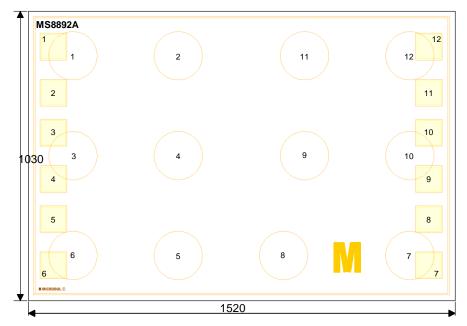


Figure 26 CSP diagram with dimensions, and alignment mark

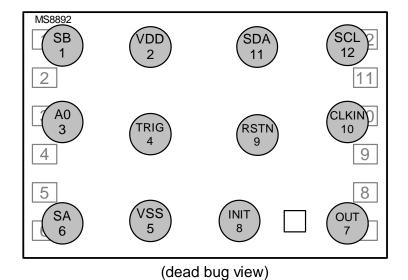


Figure 27 Signal assignment of MS8892 in final CSP package

The CSP diagrams in Figure 26 and Figure 27 have the bumps facing up ("dead bug" view).

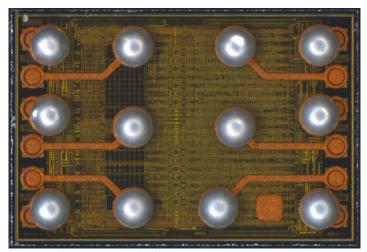


Figure 28 Photograph of MD450 CSP (different product, same ball coordinates as MS8892)

## 4.4.2.2 PCB design for the CSP package

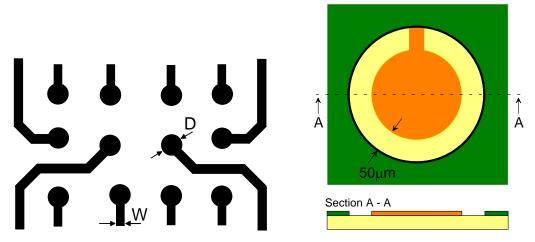


Figure 29 CSP PCB footprint and solder mask design

Symbol	Description	Value	Tolerance	Unit
D	Pad diameter	220	±20	μm
W	Width of pad connection	100 200		μm

Table 21 CSP BCP footprint dimensions

It is recommended to use a non-solder mask defined (NSMD) layout for the PCB pads with a distance of 50µm between the PCB pad and the edge of the solder mask opening.

## 4.4.3 Capacitance sensor trace design

In addition to the MS8892 IC, the capacitive sensor also consists of the physical sensor electrodes. This Section gives some background and basic guidelines for the successful implementation of the sensor electrodes in AMANDA and other applications of the MS8892.

#### 4.4.3.1 Trace design basics

Many parameters define the sensor's capacitance value and its sensitivity. It is therefore not possible to give exhaustive design guidelines. The following design guidelines are meant as a starting point for the application specific sensor design.

Figure 30 shows a simple but effective sensor layout. The sensor capacitor has two electrical conductors SA and SB. SA is the transmitter and SB is the receiver. The transmitter SA surrounds the receiver as much as possible. This gives the highest capacitance and also the highest immunity to noise. The sensor's capacitance is increased by increasing the sensor's antenna length *lb*. The sensor's capacitance is also increased by lowering the distance *d* between the transmitter and the receiver and by increasing the SA and SB conductor widths *wa* and *wb*.

It is important to shield (e.g. with VSS lines and/or a VSS grid) the receiver antenna between the MS8892 pins and the sensor area. The shielding capacity must not exceed 5pF. If properly shielded, the sensor is only sensitive at the sensor area and the capacitance is defined by the sensor area.

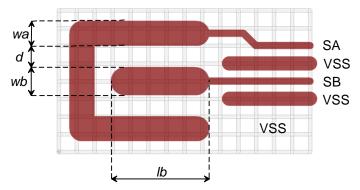


Figure 30 Example sensor trace layout

Figure 31 shows the typical sensor's relative capacitance value as a function of the distance to an object. The sensor capacitance is changed if an object (e.g. finger) is approaching the sensor area. The relation between the sensor capacitance and the distance to the object depends on many parameters and must be evaluated in the application. The closer SA and SB are drawn (d is small), the lower becomes the relative sensitivity for objects that are distant (curve A is almost flat for large distances). A large distance d between SA and SB increases the relative sensitivity for objects at large distances (curve B is steeper than curve A for larger distances).

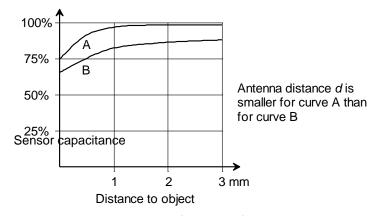


Figure 31 Sensor capacitance as a function of the distance to the object

The sensor capacitance and the relative capacitance change can be optimized with capacitance simulations of different sensor layouts, which is described in the next Section.

## 4.4.3.2 Trace design optimisation using capacitance simulation

For a given application, it is often necessary to optimise the sensor for:

- Minimal sensor area, or for a given sensor shape
- Maximal capacitance difference between touched and not touched situations, resulting in a simpler threshold setting and more robust operation
- Setting the total capacitance value well inside the allowed capacitance range
- Optimising the material choice and physical dimensions of the layer stack up (PCB, isolating overlays, housing components)

A trial and error method based on fabricating multiple prototypes is a costly and lengthy process. A capacitance simulation of the actual sensor layout combined with abstracted overlays and finger model can give a much faster initial design with good chance for successful operation and satisfactory performance. Some fine tuning may then still be done.

Microdul employs the 3-D capacitance simulation tool CapExt [15] which is specialized for capacitance simulation for capacitive touch applications.



Figure 32 Example sensor layouts captured in PCB design program (Eagle)

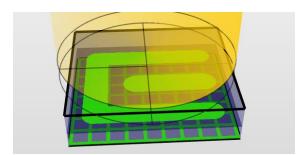


Figure 33 Trace design, loaded in capacitance simulator CapExt [15]

The transparent yellow object in Figure 34 is the model of the approaching finger. The simulation calculates capacitance values with the artificial finger present and absent. The distance of the finger from the sensor can be configured / parametrized.

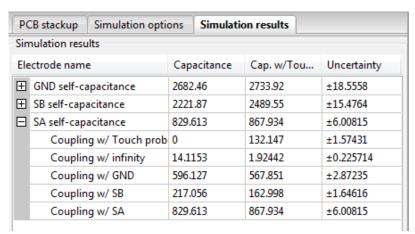


Figure 34 Example CapExt simulation results, capacitance in femtofarads

For the AMANDA ASSC card design, Microdul can support the design of the sensor electrode layout and the isolation layer stack-up with recommendations and capacitance simulations. Additionally, the new feature of the relative threshold mode allows an easier and more accurate switching threshold setting by compensation of capacitance variations due to material and manufacturing tolerances.

For the best performance of the sensor (maximizing recognition of intended touch events while reducing false positives) the following parameters have to be optimized:

- Sensor electrode layout, shielding, and isolation layer stack-up design, based on capacitance simulations
- Filter mode of the MS8892
- Threshold setting of the MS8892, using the new relative threshold mode, which compensates manufacturing tolerances

## 5 Temperature sensor

## 5.1 Objectives and requirements identified in WP1

#### 5.1.1 Conclusions from the SoA and Gap analyses

In the gap analysis in **Deliverable D1.1 - SoA and Gap analysis/recommendations on ESS features report,** it has been concluded that the most important improvement of the temperature sensor should concentrate on reducing the average power consumption at slow measurement rates further, focusing on the following three key areas:

- Reduction of measurement duration
- Reduction of current consumption during the measurement
- Reduction of static current between the measurements

Besides that, the main features of the actual temperature sensor MS1088 should be kept, for instance the bidirectional handshake line.

In the initial requirements **Deliverable D1.2 - Initial System Requirements**, the main recommendations for the temperature sensor were stated as follows:

- Supply current reduction, during both, idle mode and measurement. Average power reduction of 65% to 75%
- Reduction of the lower supply voltage limit from 2.4V to 1.8V

The supply voltage reduction to 1.8V is recommended for several reasons:

- 1.8V supply fits into the AMANDA ecosystem, where most components are powered with a lower voltage than 2.4V
- A voltage reduction directly results in a proportional reduction in power consumption, assuming unchanged supply currents
- The 1.8V level is a widely used system voltage, thus the voltage reduction increases the available market for the temperature sensor

# 5.1.2 Summary of the temperature sensor requirements and deviations from the initial plan LORA ... BLE FRAM ..... 2.2V Power Control

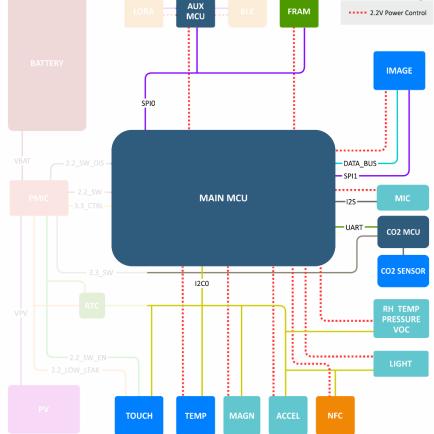


Figure 35 Place in the architecture of the temperature sensor

The main achievement of the MS1089 temperature sensor is the supply voltage reduction from 2.4V to 1.8V, while maintaining its excellent low power consumption. The initial objective for the temperature sensor of reducing the average current consumption to 20nA could not be entirely achieved due to the compromises needed to reach 1.8V operation. On the other side, several parameters have been improved in the temperature sensor for AMANDA:

- The lower supply voltage limit has been reduced from 2.4V to 1.8V, which allows the sensor to be easily integrated in the AMANDA architecture with a supply level of approximately 2.2V. Additionally, the 1.8V supply is a standard system supply voltage in the market. Therefore, this improvement has additional benefit for marketing the device
- Three selectable temperature sensing resolutions have been implemented. The highest resolution allows for a more accurate factory calibration of the sensor. Using the lowest resolution leads to the shortest measurement duration and therefore to a lower measurement power consumption

#### **5.2** Sensor key specifications

#### 5.2.1 General description and main features

The integrated circuit MS1089 is a fully integrated calibrated digital low power temperature sensor with a typical temperature measurement accuracy of  $\pm 0.3$ °C. The MS1089 has an I<sup>2</sup>C interface and is available in Chip-Scale-Package (CSP).

The main features of MS1089 are:

- Serial 2-wire I<sup>2</sup>C Fast-mode Plus (1MHz) interface
- Up to 4 sensors can be addressed over the same serial bus (4 sub-addresses)
- Reset either via input pin or via I<sup>2</sup>C command
- Hardware handshake to start a temperature measurement and wake up the microcontroller when data is ready
- High accuracy: ±0.3°C from +10°C to +40°C
- Three resolutions: 0.1°C (11-bit), 0.05°C (12-bit) and 0.025°C (13-bit), selectable with  $1^2C$
- Fast measurement time: 30ms typical at 0.1°C resolution and 120ms at 0.025°C resolution
- Ultra-low current in sleep mode: only leakage
- Peak current during measurement: 70μA
- Avg. current: 68nA at 1 measurement per minute at 0.1°C resolution
- Supply range: 1.8V to 3.6V
- Available in CSP package

The application areas of the MS1089 include the following:

- Wireless sensor tags and cards
- Wearables
- Power-supply temperature monitoring
- Environmental monitoring and HVAC
- Computer peripheral thermal protection
- Notebook computers
- Phone batteries
- Battery management
- Thermostat controls

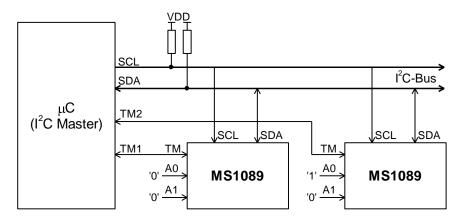


Figure 36 Typical application with two instances of the MS1089

## 5.2.2 Pin description

Pin CSP	Symbol	Туре	Description
1	RSTN	1	Reset input with internal pull-up (active LOW)
2	A1	1	User-defined I <sup>2</sup> C sub-address bit 1
3	A0	1	User-defined I <sup>2</sup> C sub-address bit 0
4	T1	I	Reserved input. Must be connected to VSS
5	T2	1	Reserved input. Must be connected to VSS

6	VSS	S	Ground
7	TM	1/0	Hardware Handshake; open-drain with internal pull-up
8	SDA	I/O	I <sup>2</sup> C-bus serial bidirectional data line; open-drain
9	SCL	1	I <sup>2</sup> C-bus serial clock input
10	VDD	S	Positive supply voltage
11	VPROG	1	Reserved input. Must be connected to VDD

Table 22 MS1089 pin description

#### Notes:

- 1. If pin RSTN is not used, can be left not connected or connected to VDD
- 2. If pin TM is not used, it must be left not connected
- 3. I<sup>2</sup>C pins SCL and SDA have no internal pull-up resistors

The pad layout of the CSP package is shown in Figure 43 on page 78.

## 5.2.3 Block diagram and basic operation

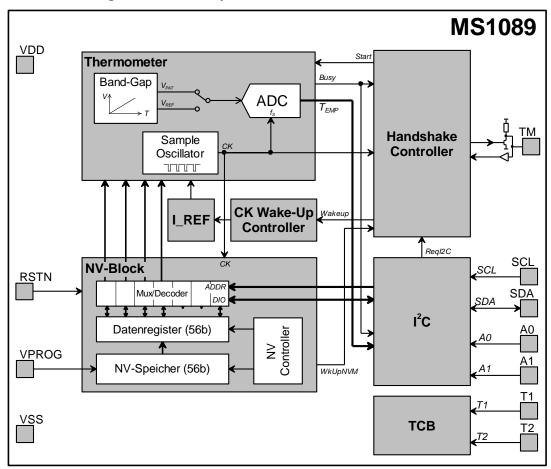


Figure 37 MS1089 block diagram

#### 5.2.3.1 Power-up and initialization

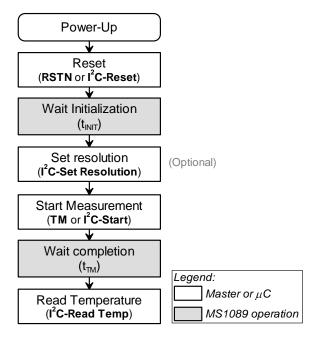


Figure 38 Operation of the MS1089

After power up, the MS1089 must be initialized with a Reset. A Reset can either be done by setting input RSTN LOW or by software with the I<sup>2</sup>C Reset command. It is strongly advised to use the RSTN pin after power-up to correctly initialize the MS1089. If not initialized with a Reset, the thermometer of the MS1089 is not calibrated and its accuracy is not guaranteed. After power-up and until a Reset is applied, the current consumption is not specified.

After a Reset pulse on RSTN or an  $I^2C$  reset command, the MS1089 performs an initialization procedure to calibrate the thermometer. After reset, the temperature measurement resolution is set to 0.1°C (11 bit). After initialization the MS1089 is on an ultra-low power state (only leakage current flows).

#### **5.2.3.2** Resolution of the thermometer

The MS1089 offers 3 selectable resolutions:  $0.1^{\circ}\text{C}$  (11 bit),  $0.05^{\circ}\text{C}$  (12 bit) and  $0.025^{\circ}\text{C}$  (13 bit). After Reset and initialization, the temperature measurement resolution of the MS1089 is set to  $0.1^{\circ}\text{C}$  (11 bit). To select a different resolution the master must send the I<sup>2</sup>C I3 write command to the MS1089.

#### Notes:

- The resolution of the thermometer can only be set while the thermometer is idle.
   While a temperature measurement is ongoing, any request for setting the resolution is ignored
- The format of the I<sup>2</sup>C-Read temperature data TD is always the same, independently of the selected resolution
- The time required for the measurement depends on the selected resolution. Therefore it also has an impact on the average current consumption I<sub>DD:AV</sub>
- The measurement resolution is not stored in non-volatile memory. Therefore, after a Power-Up or a Reset, it must always be set

#### 5.2.3.3 Temperature measurement with I<sup>2</sup>C or hardware handshake pin TM

After initialization, the MS1089 is in ultra-low power mode and ready for operation. A temperature measurement can be initiated using the I<sup>2</sup>C command I2. After completion of the

measurement TM is pulled LOW and the MS1089 returns to the ultra-low power mode. The digital value of the temperature is available in the internal register TD and can be read with the I<sup>2</sup>C command I1

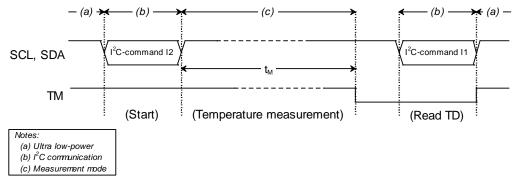


Figure 39 Temperature measurement, started with I<sup>2</sup>C

#### Notes:

- If a new I<sup>2</sup>C start measurement command (I2) is sent while a temperature measurement is on-going, the MS1089 generates no acknowledges and the command is ignored
- If an I<sup>2</sup>C read temperature command (I1) is sent while a temperature measurement is on-going, the value TD=0 (-80.000°C) is returned
- When the measurement is complete, the MS1089 pulls down pin TM until TD is read by the command I1

Temperature measurements can also be started with a pulse on the single handshake line TM, as illustrated in the following figure:

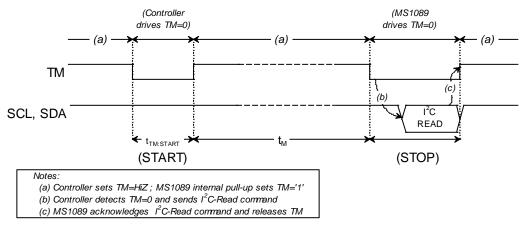


Figure 40 Temperature measurement, started with TM pulse (handshake protocol)

#### Notes:

- During the TM start pulse (T<sub>TM:START</sub>) current flows through the internal pull-up of pin TM. During the TM stop-pulse however, the MS1089 switches off its internal pull-up and therefore I<sub>DD</sub> is not affected
- If the controller generates a new LOW pulse on TM before the temperature measurement is complete and TD has been read, that pulse is ignored

	Byte 1									
D15	D14	D13	D12	D11	D10	D9	D8			
0	0	0	TD12 (MSB)	TD11	TD10	TD9	TD8			
	Byte 2									
D7	56	,	5.4	5.0						
	D6	D5	D4	D3	D2	D1	D0			

Table 23 Data format of the digital temperature value TD

The digital temperature value TD is placed in the lowest 13 bits (D12..D0) of the 2 data bytes returned by command I1. Bits D15..D13 are always 0. The digital temperature value can be converted to degree Celsius or Fahrenheit with the following formulae:

$$T (^{\circ}C) = \frac{TD}{40} - 80$$
$$T (^{\circ}F) = \left(\frac{TD}{40} - 80\right) \times 1.8 + 32$$

The formulae are correct in all resolution settings, as the MSB of the measurement is always assigned to bit D12. In 12-bit resolution setting, the lowest bit TD0 is always 0. In 11-bit resolution setting, the two lowest bits TD1, TD0 are always 0.

# 5.2.4 I<sup>2</sup>C Interface and register description

The MS1089 has a slave receiver/transmitter  $I^2C$  interface compatible with 1MHz SCL frequency. Pin SCL is clock and pin SDA are data input/output. Both pins SDA and SCL are not electrically connected to the internal supply voltage of the MS1089. They can therefore be driven to a voltage that is different than  $V_{DD}$ .

The 7-bit I<sup>2</sup>C slave address of the MS1089 consists of five fixed bit values A6 to A2 and two selectable bits A1 and A0, defined by the digital inputs A1 and A0. This allows independent operation of up to four MS1089 on the same I<sup>2</sup>C bus, with the addresses 0x48 to 0x4b.

Bit	A6	A5	A4	А3	A2	A1	A0
Value	1	0	0	1	0	A1	Α0

Table 24 MS1089 I<sup>2</sup>C address definition

#### 5.2.4.1 I<sup>2</sup>C command description

Bit	<b>C7</b>	C6	C5	C4	СЗ	C2	C1	CO
Value	0	0	0	0	0	0	C1	CO

Table 25 I<sup>2</sup>C command byte

Com- mand	C1	CO	R W	Туре	Data	Description
I1	0	0	1	2-Byte	TD = D15D0	Read temperature value TD

12	0	1	0	0-Byte	-	Start a temperature measure- ment
13	1	0	0	1-Byte	D1,D0 = 00 (11 Bit) D1,D0 = 01 (12 Bit) D1,D0 = 1X (13 Bit)	Set measurement resolution
			1	1-Byte	Res = D1,D0	Read measurement resolution
14	1	1	0	0-Byte	-	Chip reset

Table 26 I<sup>2</sup>C command table

Note: Bits C7 to C2 must always be 0. Sending commands with any of these bits set to 1 can lead to malfunction of the MS1089.

## 5.2.5 DC and AC characteristics

Conditions: V<sub>DD</sub> = 2.2V, T = 25°C; unless otherwise specified

Symbol	Parameter	Min	Тур	Max	Unit
V <sub>DD</sub>	Positive supply voltage	1.8		3.6	V
I <sub>DD</sub>	Standby operating current		33		nA
	Operating current during temperature measurement		70		μΑ
I <sub>DD:AV</sub>	Avg. operating current, 11-bit (0.1°C)		68		nA
(note 1)	Avg. operating current, 12-bit (0.05°C)		102		nA
	Avg. operating current, 13-bit (0.025°C)		172		nA
I <sub>DD:INIT</sub>	Operating current during initialization		33		μΑ
C <sub>load</sub>	Load capacitance at pin TM			10	pF
$R_{PU}$	Internal pull-up on pins TM and RSTN		124		kΩ
I <sub>SDA:OL</sub>	Low-level sink current of SDA $V_{OL} = 0.4V$	18.5			mA
T <sub>Error</sub> (note 2)	Temperature error, T = 10 °C to 40 °C		±0.3	±0.5	°C
T <sub>RES</sub>	Sensor Resolution, 11-bit		0.1		°C
	Sensor Resolution, 12-bit		0.05		°C
	Sensor Resolution, 13-bit		0.025		°C
T <sub>PSVD</sub>	Power supply voltage dependency		±0.1		°C/V
T <sub>amb</sub>	Operating temperature range	-40	25	85	°C

Table 27 Selected MS1089 DC characteristics

#### Notes:

- ullet Considering one temperature measurement every 60 seconds. Note that the average operating current increases with the measurement time  $t_M$ , which depends on the measured temperature
- The thermometer of the MS1089 is calibrated at the supply voltage of 2.2V. The temperature error T<sub>Error</sub> is specified for that supply voltage

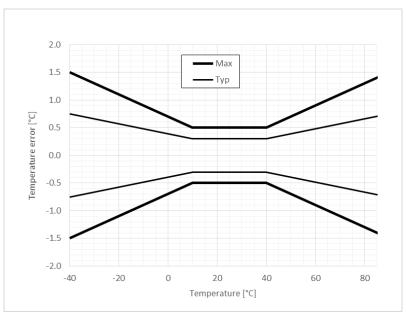


Figure 41 Temperature accuracy at 22°C

Conditions: V<sub>DD</sub> = 2.2V, T = 25°C; unless otherwise specified

Symbol	Parameter	Min	Тур	Max	Unit
t <sub>INIT</sub>	Initialization time after Reset		2		ms
t <sub>TM:START</sub>	Length of start LOW pulse at pin TM	50			ns
t <sub>RSTN</sub>	Length of Reset pulse	20			ns
t <sub>M</sub>	Temp. measuring time, 11-bit		30		ms
	Temp. measuring time, 12-bit		60		ms
	Temp. measuring time, 13-bit		120		ms
f <sub>SCL</sub> (note 1)	I <sup>2</sup> C clock frequency	0		1000	kHz

Table 28 Selected MS1089 AC characteristics

#### Notes:

• The detailed I<sup>2</sup>C timings are compliant with the 1MHz fast-mode plus standard described in the "I<sup>2</sup>C-bus specification and user manual" [16].

# 5.3 Temperature sensor evaluation

# 5.3.1 Planning

First packaged prototype samples will be available in the second half of September 20 (M21). First evaluation results are expected by the end of M20. The full evaluation is planned in the following months.

Event	Planned for	Comments
Wafer delivery	25.08.20	The wafers were delayed due to cyber-attack on the wafer foundry, but they have now arrived at Microdul (on 28.08.20).

		For the following steps, Microdul is no longer dependent on external suppliers, and the following steps can progress as planned below.	
Wafer grind and saw	05.09.20	1 wafer will be sawn for prototype packaging.	
Prototype package assembly	15.09.20	Die and wire bonding of the devices into the SOIC-16 package at Microdul	
First quick evaluation	30.09.20	A first quick evaluation based on simple lab hardware is planned before the end of M21	
Complete evaluation	31.12.20	The complete evaluation on dedicated lab hardware is planned for the end of M24	

Table 29 Sample production & evaluation planning of the MS1089

#### 5.3.2 First evaluation & calibration of prototypes

In order to quickly provide devices for the project, one wafer of the MS1089 will be sawn and some dies will be packaged on a SOIC16 package for the initial prototypes. These devices will not be wafer tested and the thermometer is not calibrated. They will be used for a first evaluation and to determine the calibration parameters. The first evaluation comprises:

- Functional evaluation in typical conditions (room temperature, 3.0V):
  - o I<sup>2</sup>C commands
  - TM operation
  - RSTN and initialization
- Thermometer calibration: A small number of devices (10) are measured at 2 temperatures (0°C and +30°C) on a temperature bath.
  - The linearity is set to default (CAL BG=0) and is not optimized<sup>2</sup>.
  - The Slope (CAL\_SLP) and Offset (CAL\_OFF) is computed individually for each device. This is different than later in production, during which the slope is the same for all devices and the offset is calculated at +30°C.

The remaining 2 wafers are reserved for later development of the CSP, and the industrial test program and calibration.

#### 5.3.3 Full evaluation

The full evaluation will consist of the following Tasks:

- Functional evaluation over the temperature and voltage supply range:
  - o I<sup>2</sup>C commands
  - TM operation
  - o RSTN and initialization
  - Test modes
- Thermometer calibration (12 devices, measured in a temperature bath from -40°C to +85°C):
  - Linearity optimization: determine the CAL\_BG value that results in the best linearity
  - Slope optimization: determine the best value of CAL\_SLP that results in the best accuracy when CAL\_OFF is determined at +30°C (standard temperature for industrial calibration)
- Characterization of temperature resolutions (11, 12 and 13 bit):

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<sup>&</sup>lt;sup>2</sup> Because of that, later devices may have a better linearity than the prototypes. We expect however that the linearity of the prototypes is close to the optimum.

- Accuracy
- Linearity
- Measurement time as function of the temperature and resolution
- Parametric evaluation (according the specification):
  - DC characteristics
  - AC characteristics

#### 5.3.4 Evaluation results

The evaluation results of the temperature sensor will be published in a different Deliverable, either in D2.5 - Finalised Prototypes Report or D6.2 - Characterisation/test reports of individual components in lab environment.

## 5.4 Prototype samples and final miniaturized samples

#### 5.4.1 Prototype samples

The MS1089 temperature sensor prototype samples are delivered in the same JEDEC compliant narrow SOIC-16 package [14] as used for the MS8892. The package drawing is shown in Figure 22 on page 59. The package enables a fast-track assembly of the first untested silicon dies in-house at Microdul. Additionally, the package is suitable for mounting in a standard socket for electrical and functional evaluation of the ICs. In this way, existing lab hardware can readily be reused.

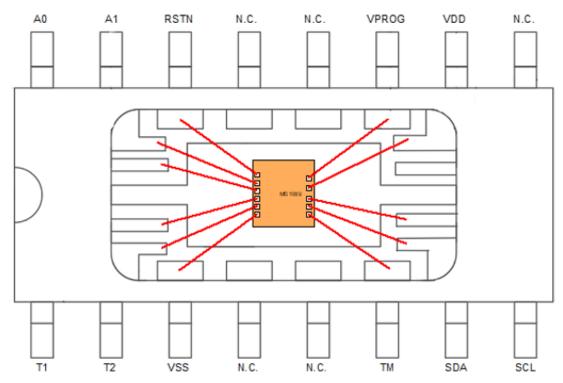


Figure 42 Bonding diagram and pin assignment of MS1089 in SOIC-16 prototype package

# 5.4.2 Final miniaturized samples for the ASSC

# 5.4.2.1 CSP specification

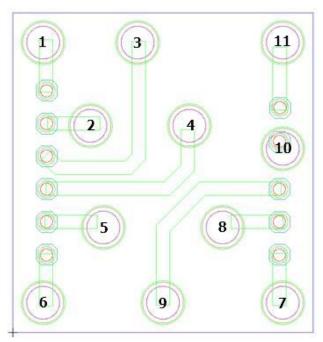


Figure 43 MS1089 CSP pad layout, the bumps facing up ("dead bug" view)

Parameter	Value
CSP X	1095μm
CSP Y	1170μm
CSP Z	837µm
Number of I/Os	11
Bump height	100μm
Bump diameter	160μm
Bump material	Sn (97.5%)
	Ag (2.5%)

Name	Bump	Ball coordinate			
		X μm	Yμm		
RSTN	1	0	0		
A1	2	172	-303		
A0	3	345	0		
T1	4	533	-303		
T2	5	220	-675		
VSS	6	0	-950		
TM	7	875	-950		
SDA	8	655	-675		
SCL	9	438	-950		
VDD	10	875	-387		
VPROG	11	875	0		
Alignment mark		tbd	tbd		

Table 30 CSP specification and solder ball coordinates of MS1089

#### Notes on Table 30:

- Solder ball co-ordinates are from the centre of the ball
- Values for CSP X and CSP Y are after sawing
- CSP Z includes the bump height (over-all height)
- Coordinates are given relative to ball 1

#### 6 Outlook

This Section presents a short outlook per sensor, mentioning topics that could not be covered sufficiently in this report due to the report schedule and the different delays encountered in the sensor developments. These delays are partly due to the complications caused by the Covid-19 situation, and partly due to unexpected technical or administrative issues.

For all four sensors, evaluation results are mostly not available at the time of completion of this report. The evaluation of the finalized sensors is part of Task T2.5 - Prototypes finalization and T6.2 - Lab Environment Validation, and will be reported in the corresponding Deliverables D2.5 - Finalised Prototypes Report, and D6.2 - Characterisation/test reports of individual components in lab environment, which are due later in the project.

#### 6.1 Imaging sensor development

EPEAS is currently waiting for the samples to come back from the fab. Measurements and delivery of samples for the PCB cannot be performed at the current time.

The remaining Tasks includes:

- Finalize the package selection
- Measurements and characterisations

#### 6.2 CO<sub>2</sub> sensor development

The CO<sub>2</sub> sensor consist of two parts: the transducer and the electronic readout. During the development of the transducer unforeseen technical difficulties appeared. A mitigation plan was implemented. For that reason, additional tests need to be executed. Different material needs to be tested. The development of the electronic readout went according to plan. However, it is expected that software adjustment to new materials will be needed.

The samples of current setup are available for tests. Power consumption communication protocol and mounting can be tested. The availability of final samples depends on results of the research. It is expected that parameters of final solution might slightly vary from current device but the difference in terms of dimensions and power consumption should be minor.

The work will continue, and the results will be reported in D2.5 at month M26 of the project.

#### 6.3 Capacitive sensor development

The development of the capacitive sensor is complete, the wafers fabricated and the sample production ongoing. First functional evaluation results are expected by the end of M20. If successful, samples for the unconstrained AMANDA ASSC prototype will be available in line with the original schedule. Therefore, the development of the capacitive sensor can be considered complete.

#### 6.4 Temperature sensor development

The development of the temperature sensor is complete, and the wafers are in fabrication. The tape out was done in time with the plan to have prototype samples in M20 of the project, assuming the predicted wafer fabrication time. Due to the previously mentioned cyber-attack, the wafer fab has however stopped the operations completely for nearly a month. Therefore, the delivery of the wafers and all following processing steps are delayed by a month.

The remaining Tasks for the completion of the temperature sensor development until the availability of prototype samples include:

- Wafer sawing, once the wafers are available (end of M20)
- Prototype assembly (die bonding, wire bonding)
- Initial functional check of the ICs
- Manual temperature calibration of the ICs to be supplied to the AMANDA prototype

The current expectation is, that the prototype samples can be delivered with one month delay in M21 (end of September 2020).

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